IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

ON SEMICONDUCTOR CORPORATION and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,	)	REDACTED-PUBLIC VERSION
Plaintiffs,	)	
v.	)	C.A. No. 17-247-LPS
POWER INTEGRATIONS, INC.,	)	[redacted]
Defendant.	)	

VOLUME 1 of 2 (A1-A669)
APPENDIX OF EXHIBITS CITED IN
POWER INTEGRATIONS, INC.'S MOTIONS FOR SUMMARY JUDGMENT

OF COUNSEL:
Douglas E. McCann
Joseph B. Warden
Warren K. Mabey, Jr.
FISH & RICHARDSON P.C.
222 Delaware Ave, 17th Floor
Wilmington, DE 19801
(302) 652-5070

Frank E. Scherkenbach
FISH & RICHARDSON P.C.
One Marina Park Drive
Boston, MA 02210
(617) 521-7883

Michael R. Headley
Howard G. Pollack
Neil A. Warren
FISH & RICHARDSON P.C.
500 Arguello Drive
Redwood City, CA 94063
(650) 839-5007

John W. Shaw (No. 3362)
Andrew E. Russell (No. 5382)
Jeff Castellano (No. 4837)
SHAW KELLER LLP
I.M. Pei Building
1105 North Market Street, 12th Floor
Wilmington, DE 19801
(302) 298-0700
jshaw@shawkeller.com
arussell@shawkeller.com
jcastellano@shawkeller.com

Attorneys for Defendant

John W. Thornburgh
FISH & RICHARDSON P.C.
12390 El Camino Real
San Diego, CA 92130
(858) 678-4312

Sabrina Wilson
FISH & RICHARDSON P.C.
1180 Peachtree Street NE
21st Floor
Atlanta, GA 30309
(404) 879-7209

Dated: August 6, 2019

TABLE OF CONTENTS

EXHIBIT 1

IPW

Attorney's Docket No.: 14225-053001 / F1040330US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Isao Ochiai et al.	Art Unit	: Unknown
Serial No.	: 10/881,561	Examiner	: Unknown
Filed	: June 30, 2004		
Title	: SEMICONDUCTOR DEVICE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT IN REPLY TO ACTION OF NOVEMBER 17, 2005

Please amend the above-identified application as follows:

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

January 17, 2006
Date of Deposit

Rose Syracuse
Signature

Rose Syracuse
Typed or Printed Name of Person Signing Certificate

Amendments to the Drawings:

The attached replacement sheets of drawings includes changes to Figs. 8-10 and replace the original sheets including those figures.

Figs. 8-10 have been labeled with the designation "Prior Art" as required by the Examiner.

Attachments following last page of this Amendment:

Replacement Sheets (2 pages)

REMARKS

Applicant thanks the Examiner for allowing claims 1-8.

The claims and specification have been amended to change the phrase "seal resin" to "sealing-resin."

Also, claim 5 has been amended to recite a "plurality" of leads and a "plurality" of common leads. Those features were recited in claim 1 as originally filed.

Minor amendments to claims 2 and 6 have been made by deleting the word "when" and by adding the word "and."

As required by the Examiner, figures 8-10 have been labeled as "Prior Art."

Applicant submits that the application is in condition for allowance and respectfully requests such favorable action.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

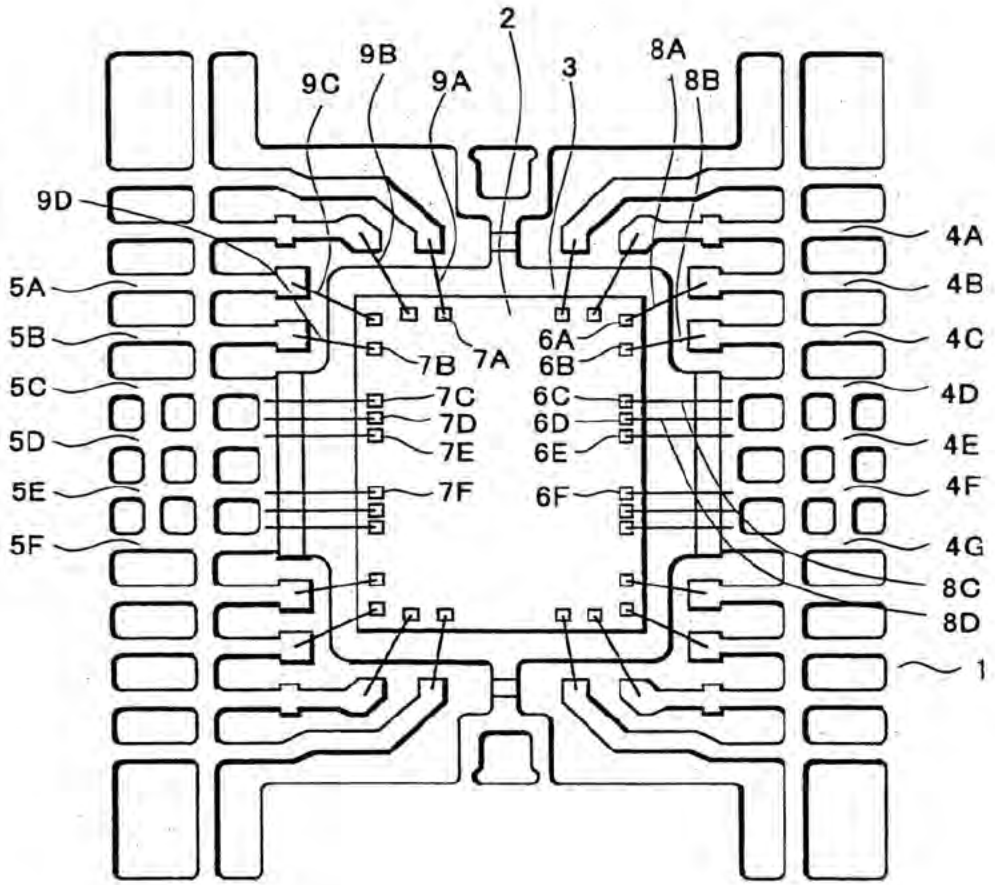
Date: 1/17/06

Samuel Borodach
Reg. No. 38,388

Fish & Richardson P.C.
Citigroup Center
52nd Floor
153 East 53rd Street
New York, New York 10022-4611
Telephone: (212) 765-5070
Facsimile: (212) 258-2291

30263459.doc

FIG.8



PRIOR ART

FISH & RICHARDSON P.C.

45 Rockefeller Plaza
Suite 2800
New York, New York
10111

Telephone
212 765-5070

Facsimile
212 258-2291

Web Site
www.fr.com

Frederick P. Fish
1855-1930

W.K. Richardson
1859-1951

June 30, 2004

Attorney Docket No.: 14225-053001

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Presented for filing is a new original patent application of:

Applicant: ISAO OCHIAI AND MASATO TAKE

Title: SEMICONDUCTOR DEVICE

FR

BOSTON
DALLAS
DELAWARE
NEW YORK
SAN DIEGO
SILICON VALLEY
TWIN CITIES
WASHINGTON, DC

Enclosed are the following papers, including those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	13
Claims	2
Abstract	1
Declaration	[To be Filed at a Later Date]
Drawing(s)	8

Enclosures:

— A certified copy of the priority application will be filed at a later date.
— Postcard.

Under 35 USC 119, this application claims the benefit of a foreign priority application filed in Japan, serial number 2003-189633, filed July 1, 2003.

Basic filing fee	$770
Total claims in excess of 20 times $18	$0
Independent claims in excess of 3 times $86	$0
Fee for multiple dependent claims	$0
Total filing fee:	$770

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EF045061733US

June 30, 2004
Date of Deposit

ONSemi-De0000609

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (212) 765-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please direct all correspondence to the following:

26211
PTO Customer Number

Respectfully submitted,

Samuel Borodach
Reg. No. 38,388
Enclosures
SXB/gzm
30194754.doc

【図８】

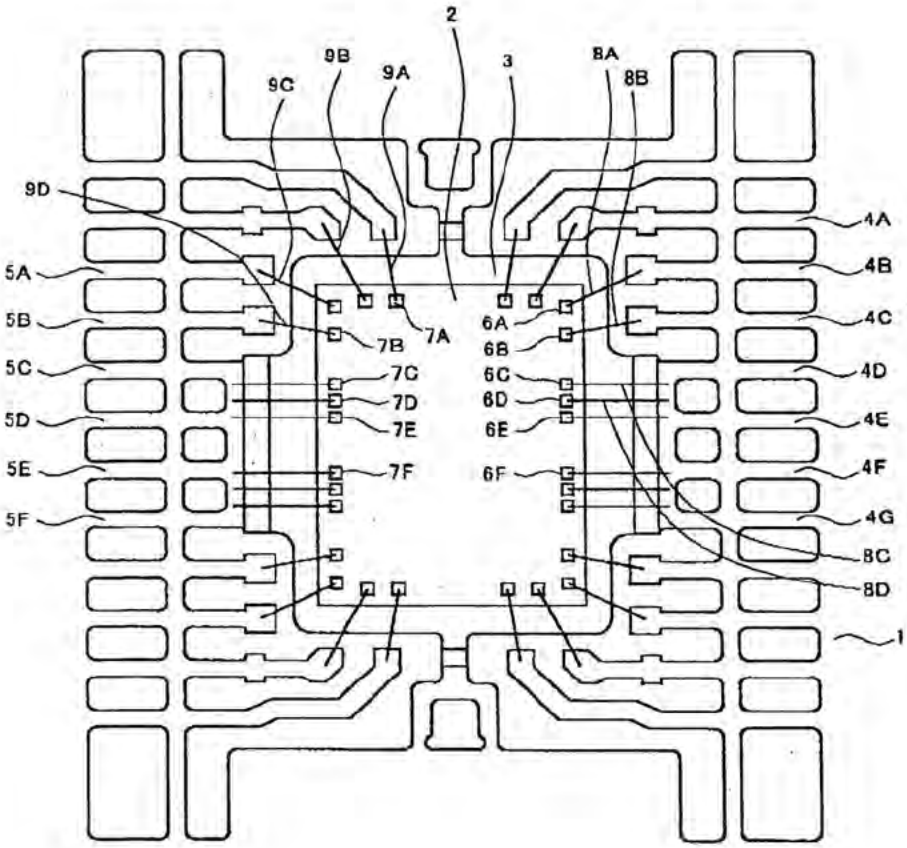

2
9B
9A
3
8A
9C
8B
9D
4A
5A
4B
5B
6A
4C
7B
7A
6B
5C
7C
6C
4D
7D
6D
5D
7E
6E
4E
5E
7F
6F
4F
5F
4G
8C
8D
1

EXHIBIT 2

REDACTED IN ITS ENTIRETY

EXHIBIT 3

(12) **United States Patent**
Ochiai et al.

(10) **Patent No.: US 7,102,211 B2**
(45) **Date of Patent: Sep. 5, 2006**

(54) **SEMICONDUCTOR DEVICE AND HYBRID INTEGRATED CIRCUIT DEVICE**

(75) Inventors: **Isao Ochiai**, Gunma (JP); **Masato Take**, Saitama (JP)

(73) Assignees: **Sanyo Electric Co., Ltd.**, Osaka (JP); **Kanto Sanyo Semiconductors Co., Ltd.**, Gunma (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/881,561**

(22) Filed: **Jun. 30, 2004**

(65) **Prior Publication Data**

US 2005/0236706 A1 Oct. 27, 2005

(30) **Foreign Application Priority Data**

Jul. 1, 2003 (JP) ..... P. 2003-189633

(51) **Int. Cl.**
H01L 23/495 (2006.01)

(52) **U.S. Cl.** **257/666**; 257/672; 257/695; 257/696

(58) **Field of Classification Search** ..... 257/666, 257/672, 674, 676, 677, E23.049; 438/123, 438/FOR. 365, FOR. 366, FOR. 380, 110, 438/111; 613/813
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,482,915 A * 11/1984 Nishikawa et al. 257/669
5,495,125 A * 2/1996 Uemura 257/666
5,903,050 A * 5/1999 Thurairajaratnam et al. 257/695

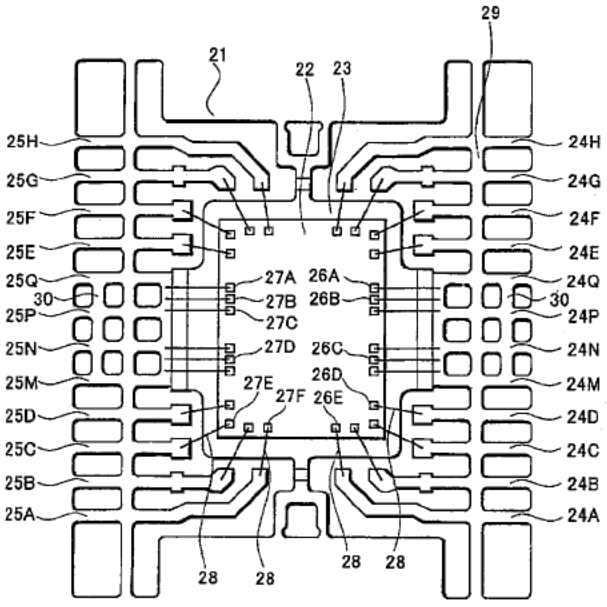
* cited by examiner

Primary Examiner—Jasmine Clark
(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

The related arts have difficulty in efficiently dissipating the heat generated by a resin-molded semiconductor element, and thus have the problem of thermal stress causing damage to the semiconductor element. To solve the problem, a semiconductor device of the preferred embodiments includes common leads coupled to an island, and a part of the common leads projects out from a resin seal body. The projecting common leads have a coupling portion. When mounting the semiconductor device, the common leads are bridged with brazing material. Thus, the heat generated by an integrated circuit chip mounted on the island is dissipated through the common leads to the outside of the resin seal body. In the preferred embodiments of the invention, a further improvement in heat dissipation characteristics can be accomplished by increasing the surface areas of the common leads.

12 Claims, 8 Drawing Sheets



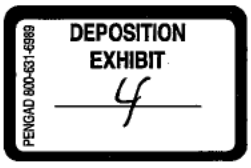


FIG. 1

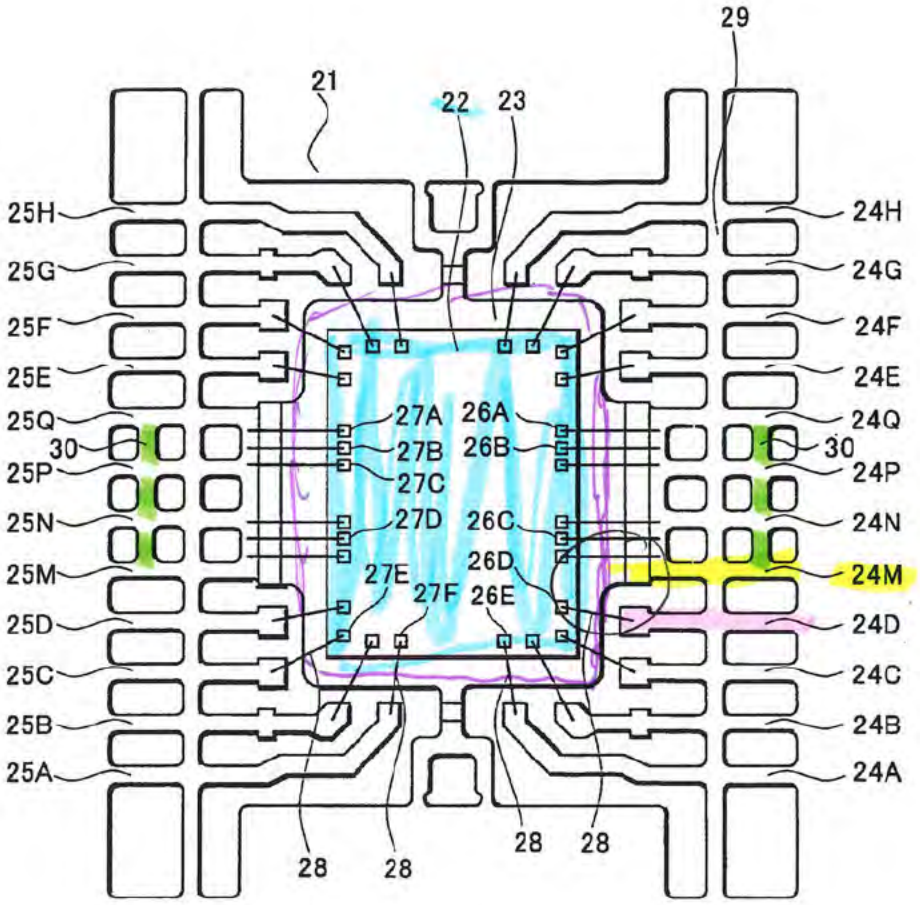

29
21
22
23
25H
25G
25F
25E
25Q
30
25P
25N
25M
25D
25C
25B
25A
24H
24G
24F
24E
24Q
30
24P
24N
24M
24D
24C
24B
24A
27A
26A
27B
26B
27C
27D
26C
26D
27E
27F
26E
28
28
28
28

FIG.2

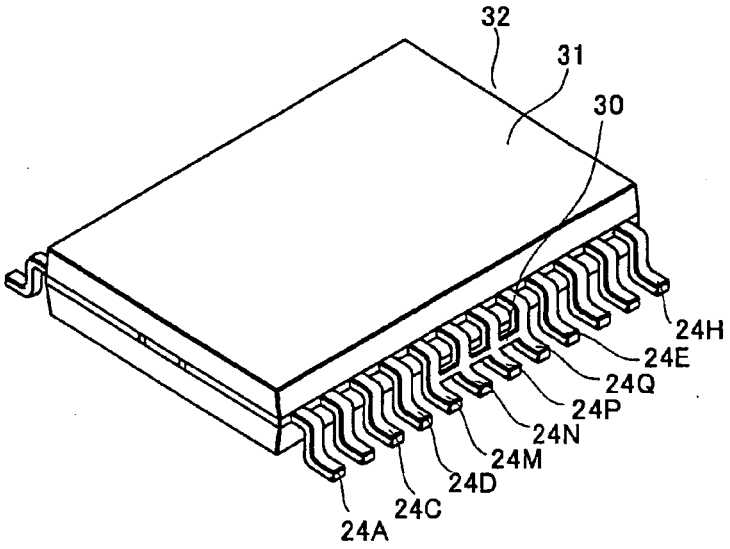

32
31
30
24H
24E
24Q
24P
24N
24M
24D
24C
24A

FIG.3

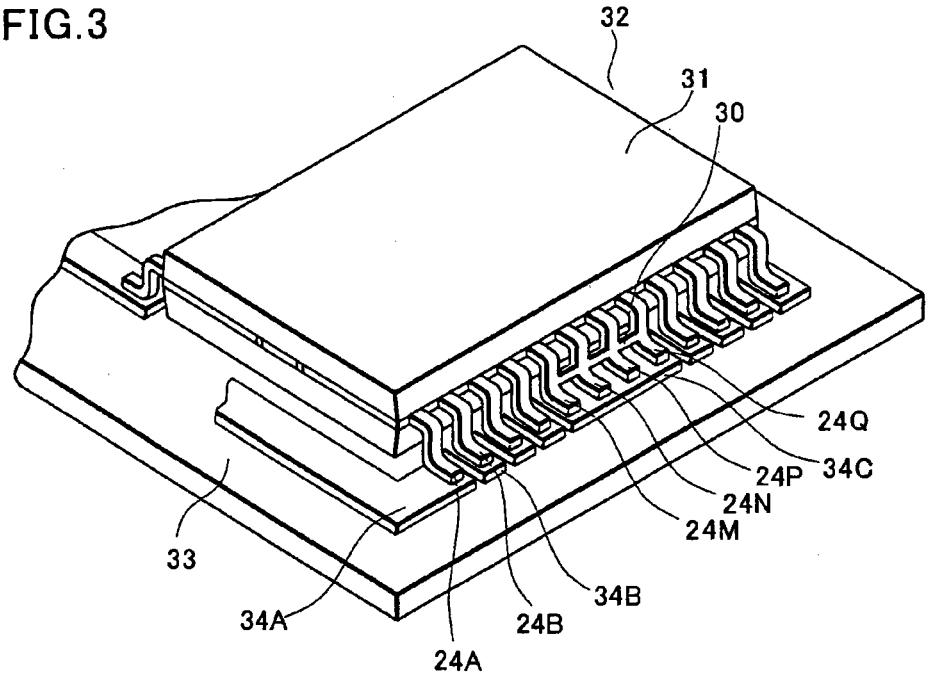

32
31
30
24Q
24P
34C
24N
24M
33
34B
34A
24B
24A

FIG.4

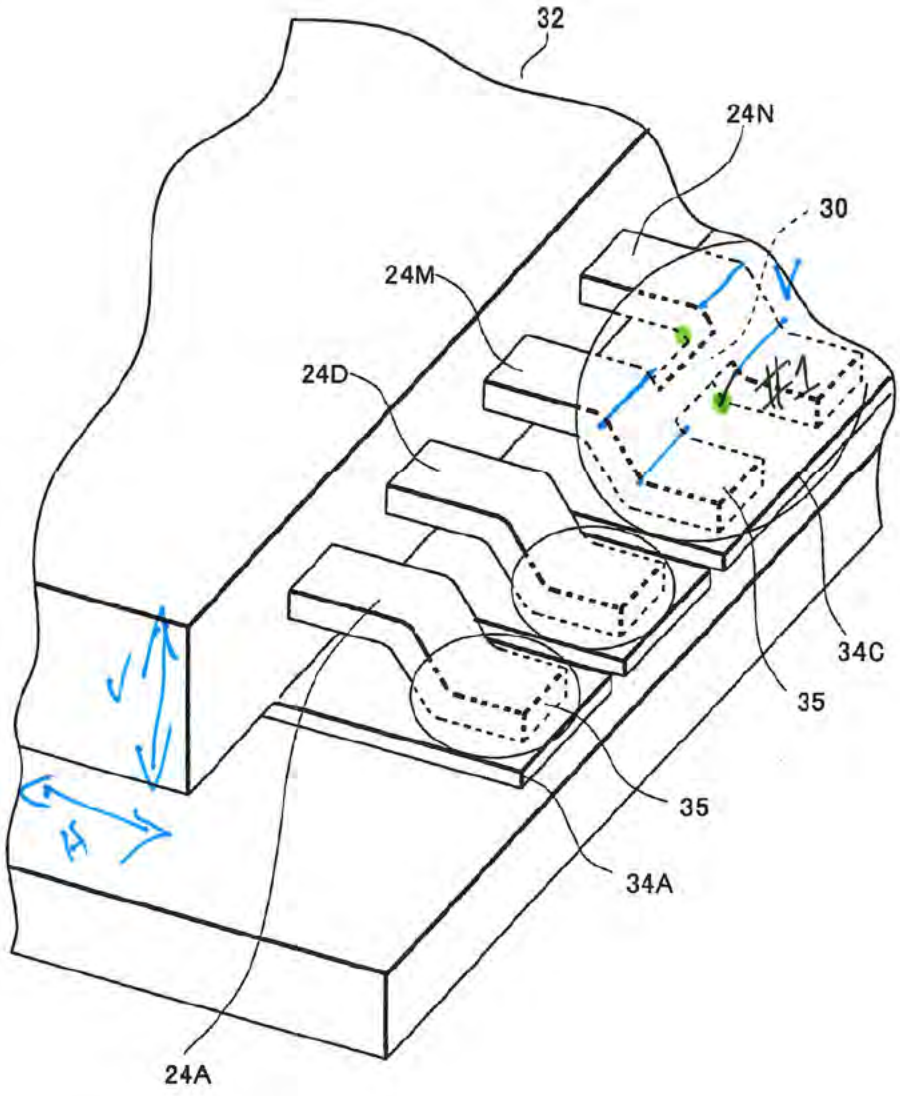


FIG.5A

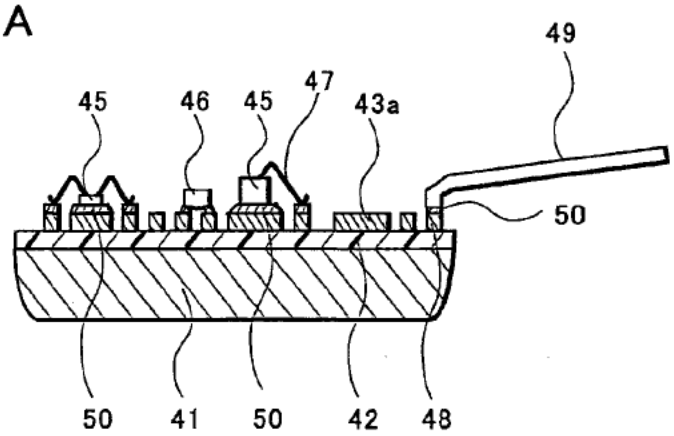

49
45
46
45
47
43a
50
50
41
50
42
48

FIG.5B

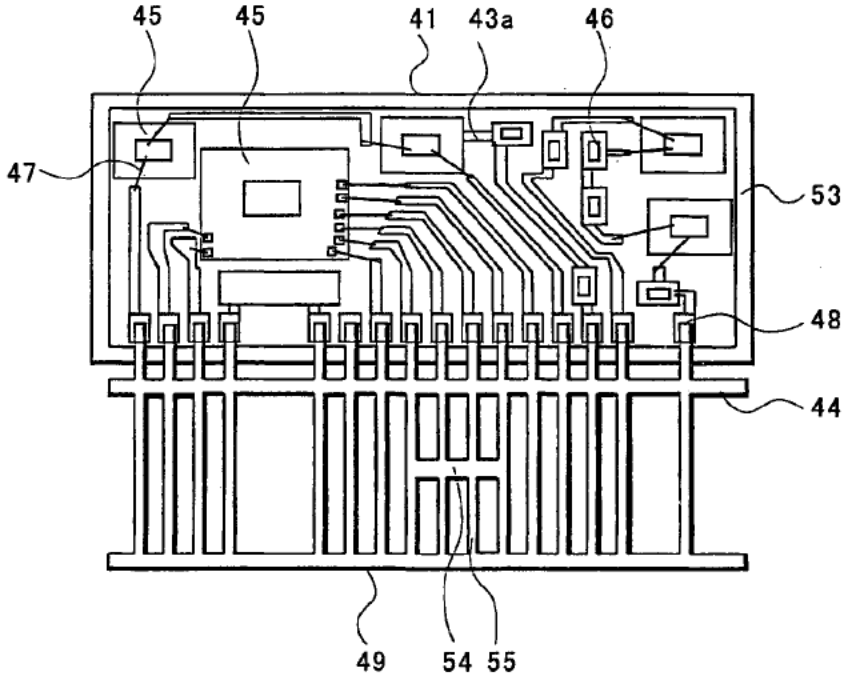

45
45
41
43a
46
47
53
48
44
49
54
55

FIG.6A

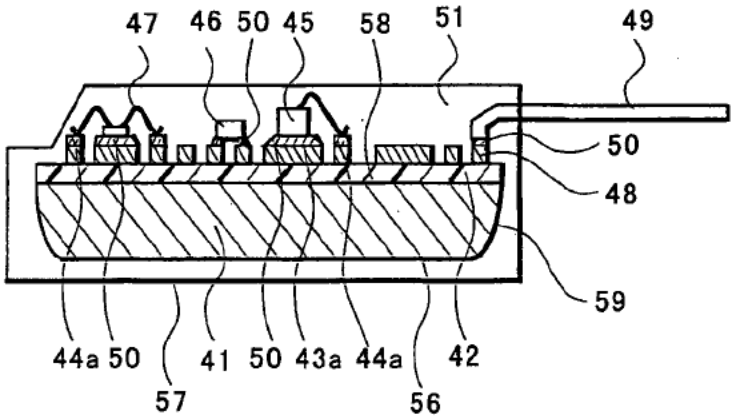
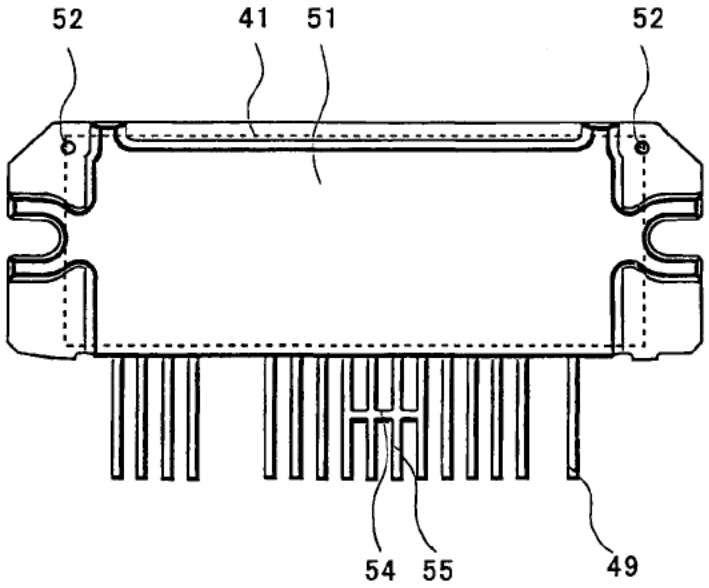

47
46
50
45
58
51
49
50
48
59
44a
50
57
41
50
43a
44a
56
42

FIG.6B


52
41
51
52
54
55
49

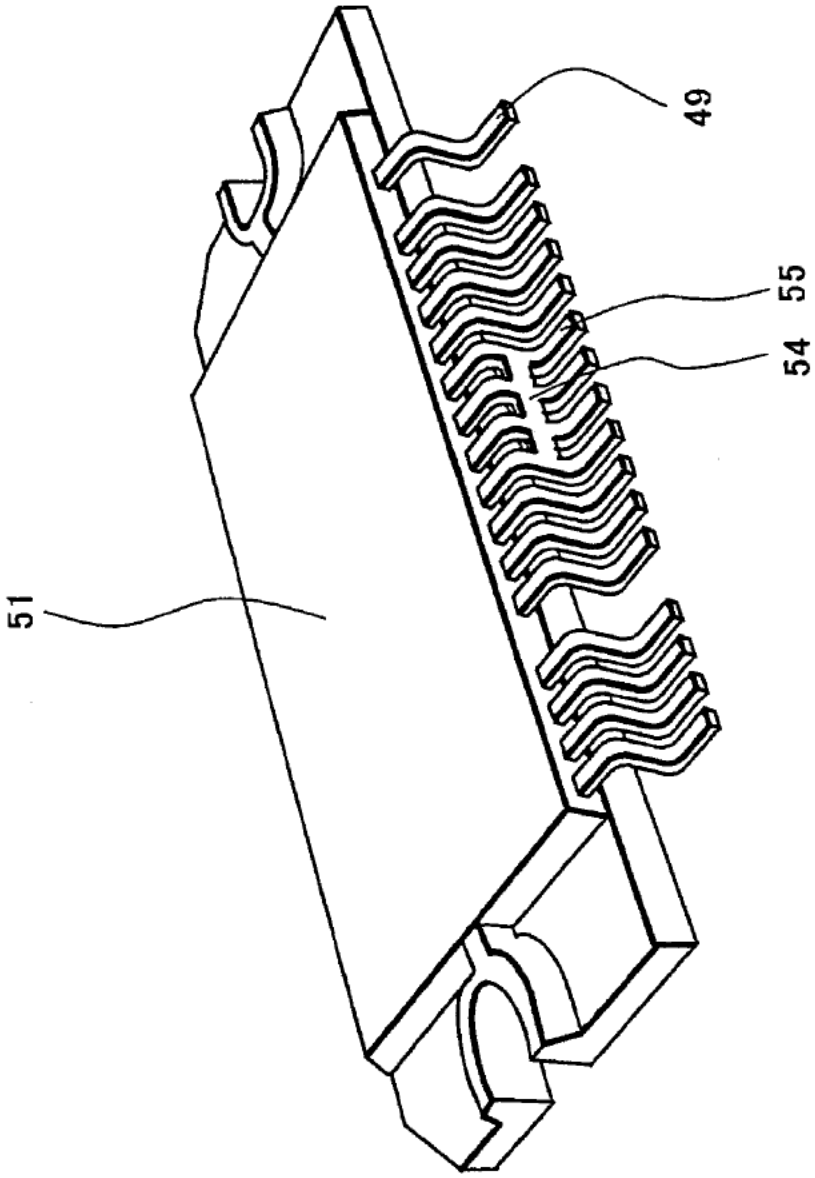
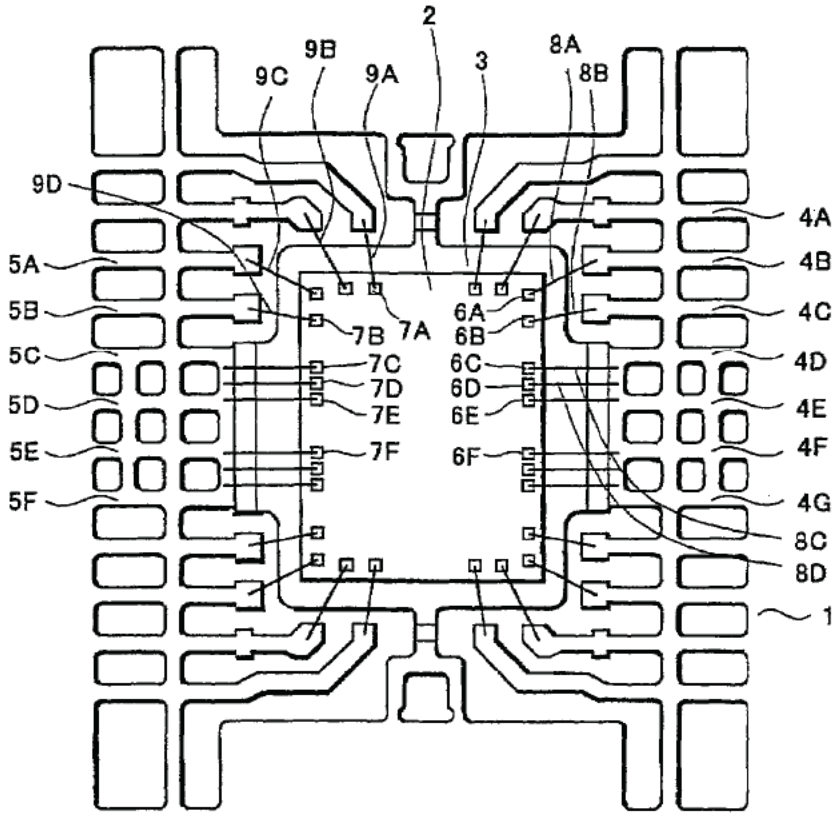


FIG.7

FIG.8



PRIOR ART

FIG.9

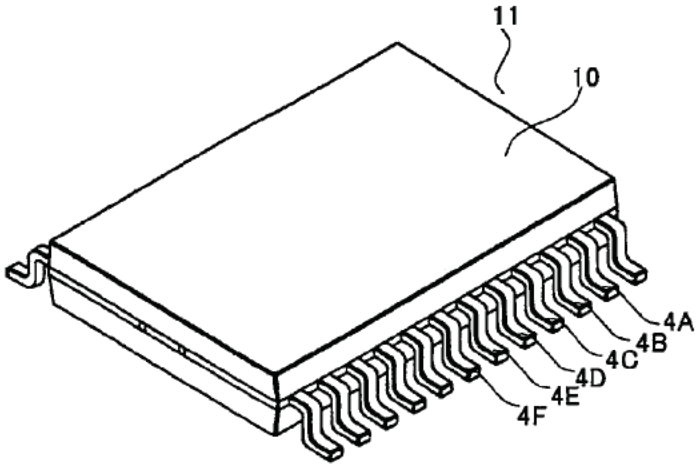
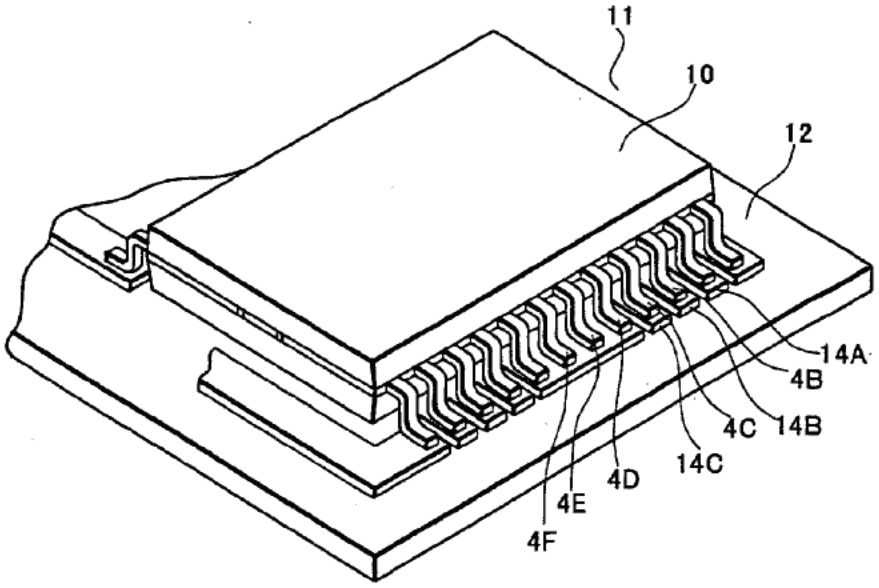


FIG.10



PRIOR ART

SEMICONDUCTOR DEVICE AND HYBRID INTEGRATED CIRCUIT DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device using a lead frame including discrete leads and common leads, and more particularly to a semiconductor device including common leads of which outer portions have a coupling portion and which are bridged with brazing material (e.g., solder or the like) in order to enhance a heat dissipation effect.

2. Description of the Related Art

Recently, higher-density semiconductor devices have been sought in order to comply with smaller-sized electronic equipment. Thus, an approach has been carried out, which involves mounting on a lead frame an integrated circuit chip having various LSI (large scale integrated) circuits, and encapsulating with resin the integrated circuit chip mounted on the lead frame.

The description is given with regard to a conventional semiconductor device with reference to FIGS. **8** to **10**.

FIG. **8** is a plan view of a conventional lead frame having an integrated circuit chip mounted thereon. FIG. **9** is a perspective view of a semiconductor device using the lead frame. FIG. **10** is a perspective view of the semiconductor device using the lead frame as mounted on a conductive pattern.

As shown in FIG. **8**, a lead frame **1** includes an island **3** on which an integrated circuit chip **2** is mounted, and a plurality of leads **4**A, **4**B, **4**C, . . . , and **5**A, **5**B, **5**C, . . . , which act as external electrode terminals. The leads **4**A and the like are arranged in DIP (dual in-line package) form and spaced at predetermined intervals.

The integrated circuit chip **2** is mounted on the island **3** of the lead frame **1**. Electrodes **6**A, **6**B, **6**C, . . . , and **7**A, **7**B, **7**C, . . . placed on the integrated circuit chip **2** are respectively bonded to the leads **4**A and the like through fine metal wires **8**A, **8**B, **8**C, . . . , and **9**A, **9**B, **9**C, . . .

As shown in FIG. **9**, a resin-sealing body **10** is formed so that the outer portions of the leads **4**A and the like are exposed to the outside thereof, and thus a semiconductor device **11** is completed.

As shown in FIG. **10**, in the semiconductor device **11**, the ends of the leads **4**A and the like are brazed (e.g., soldered or otherwise bonded) to conductive patterns **14**A, **14**B, **14**C, and the like on a printed wiring board **12**.

As mentioned above, the semiconductor device includes the integrated circuit chip, which is increasing in size year by year. Thus, the heat generated by the integrated circuit chip and the like can cause thermal damage to the integrated circuit chip or the semiconductor device. Although it is therefore necessary to improve heat dissipation characteristics of the semiconductor device, the semiconductor device has the problem of inadequate heat dissipation because the integrated circuit chip and the island having the chip mounted thereon are integrally molded with resin. Moreover, the lead frame having a larger number of pins becomes thinner and thus there was the problem of impairing the heat dissipation characteristics.

SUMMARY OF THE INVENTION

The preferred embodiments of the present invention are designed to overcome the foregoing problems. A semiconductor device of the preferred embodiments includes: an island on which a semiconductor element is mounted; a plurality of discrete leads of which ends extend near the island; a plurality of common leads coupled to the island; and a resin-sealing body molding the semiconductor element, the island, the discrete leads, and the common leads with resin, wherein the common leads projecting out from the resin-sealing body are provided with a coupling portion. With this structure, the semiconductor device can dissipate the heat through the common leads coupled to the island to the outside of the resin-sealing body. Therefore, heat dissipation characteristics of the semiconductor device can be improved.

Moreover, a hybrid integrated circuit device of the preferred embodiments includes: a conductive pattern formed at least on a surface of a hybrid integrated circuit board; a semiconductor element or a passive element mounted on the conductive pattern; a lead connected to the conductive pattern and extending outside, the lead acting as an output or an input; and a resin-sealing body made of thermosetting resin, which coats at least the surface of the board by transfer molding, wherein the lead has common leads in its region projecting out from the resin-sealing body, and the common leads are coupled by a coupling portion. With this structure, the hybrid integrated circuit device including the transfer-molded hybrid integrated circuit board can dissipate the heat to the outside of the resin-sealing body. Therefore, heat dissipation characteristics of the hybrid integrated circuit device can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view explaining a lead frame for use in a semiconductor device according to a first embodiment of the present invention;

FIG. **2** is a perspective view explaining the semiconductor device according to the first embodiment of the invention;

FIG. **3** is a perspective view explaining the semiconductor device according to the first embodiment of the invention as mounted on a conductive pattern;

FIG. **4** is an enlarged partial perspective view of the semiconductor device according to the first embodiment of the invention as mounted on the conductive pattern;

FIGS. **5**A and **5**B are a cross-sectional view and a plan view, respectively, explaining a hybrid integrated circuit board according to a second embodiment of the invention;

FIGS. **6**A and **6**B are a cross-sectional view and a plan view, respectively, explaining a hybrid integrated circuit device according to the second embodiment of the invention;

FIG. **7** is a perspective view explaining the hybrid integrated circuit device according to the second embodiment of the invention;

FIG. **8** is a plan view explaining a lead frame for use in a conventional semiconductor device;

FIG. **9** is a perspective view explaining the conventional semiconductor device; and

FIG. **10** is a perspective view explaining the conventional semiconductor device as mounted on a conductive pattern.

DETAILED DESCRIPTION OF THE INVENTION

Firstly, the description is given with reference to FIGS. **1** to **4** with regard to a semiconductor device according to a first embodiment of the present invention.

FIG. **1** is a plan view explaining a lead frame for use in this embodiment. FIG. **2** is a perspective view explaining the

semiconductor device according to this embodiment. FIG. **3** is a perspective view explaining the semiconductor device according to this embodiment as mounted on a conductive pattern. FIG. **4** is an enlarged partial perspective view of the semiconductor device according to this embodiment as mounted on the conductive pattern.

As shown in FIG. **1**, a lead frame **21** includes an island **23** on which an integrated circuit chip **22** is mounted, a plurality of discrete leads **24**A, **24**B, **24**C, . . . , and **25**A, **25**B, **25**C, . . . , which act as external electrode terminals, and a plurality of common leads **24**M, **24**N, **24**P, **24**Q, **25**M, **25**N, **25**P, and **25**Q, which are coupled to the island **23**.

The island **23** is located in the center of the lead frame **21**. A plurality of discrete leads **24**A and the like, and a plurality of common leads **24**M and the like are arranged in DIP form and spaced at predetermined intervals on both sides of the island **23**. The common leads **24**M and the like have one ends coupled to the island **23**, and the other ends which extend to the outside of the island **23** so as to act as outer portions. The common leads **24**M and the like are arranged adjacently to one another in the center of arrays of leads located on both sides of the island **23**. The discrete leads **24**A and the like are arranged on both sides of arrangements of the common leads **24**M and the like, and the number of discrete leads arranged on one sides of the arrangements of the common leads is the same as the number of discrete leads arranged on the other sides thereof.

In this embodiment, coupling portions **30** are used to connect the outer portions of the common leads **24**M and the like. Generally, tie bars **29** are used to couple the common leads **24**M and the like and couple the discrete leads **24**A and the like, so that the tie bars **29** prevent resin from leaking when resin molding is performed. In this embodiment, the coupling portions **30** are located at the middle positions between the tie bars **29** and the ends of the common leads **24**M and the like. Since the common leads **24**M and the like have one ends coupled to the island **23**, the common leads have a common potential (i.e., a ground potential) as viewed in terms of electric potential. Hence, the presence of the coupling portions **30** causes no problem in using the semiconductor device.

The integrated circuit chip **22** is mounted on the island **23** of the above-mentioned lead frame **21** with a conductive adhesive such as silver paste. Many electrodes **26**A, **26**B, **26**C, . . . , and **27**A, **27**B, **27**C, . . . placed on the integrated circuit chip **22** are bonded to the discrete leads **24**A and the like through fine metal wires **28**. Electrodes **26**M, **26**N, . . . , and **27**M, **27**N, . . . having a ground potential are bonded to the common leads **24**M and the like through the fine metal wires **28**.

Then, by transfer molding, the lead frame **21**, the integrated circuit chip **22**, and the inner portions of the leads are molded with resin, thereby forming a resin-sealing body **31**. After molding, the tie bars **29** are cut off so that the discrete leads **24**A and the like are electrically independent. Therefore, the common leads **24**M and the like are coupled by the coupling portions **30**.

As shown in FIG. **2**, the discrete leads **24**A and the like, and common leads **24**M and the like which project out from both sides of the resin-sealing body **31**, are each curved and formed into a gull-wing shape. In this case, the coupling portions **30** are located in the vertical portions of the common leads **24**M and the like.

As shown in FIG. **3**, in a completed semiconductor device **32**, the discrete leads **24**A and the like, and common leads **24**M and the like, which project out from the resin-sealing body **31**, are bonded to corresponding conductive patterns **34**A, **34**B, **34**C, . . . on a printed wiring board **33** with brazing material (e.g., solder or the like).

As shown in FIG. **4**, when bonding is performed, plenty of conductive adhesive, such as brazing material (e.g., solder or the like) **35**, adheres to the curved portions of the common leads **24**M and the like coupled by the coupling portions **30**. Thus, the brazing material (e.g., solder or the like) **35** adheres to space between the common leads **24**M and the like with the coupling portions **30** therebetween, so that the common leads **24**M and the like are bridged with the brazing material (e.g., solder or the like) **35**. This is accomplished by utilizing the surface tension of the brazing material (e.g., solder or the like) **35**. The space between the common leads **24**M and the like is filled with the brazing material (e.g., solder or the like) **35**, so that the common leads **24**M and the like function as a large lead.

With this structure, the common leads **24**M and the like have a large surface area and a great thickness. Thus, the heat generated by the integrated circuit chip **22** is transferred from the island **23** to the common leads **24**M and the like, which are bridged with the brazing material (e.g., solder or the like) **35**. Then, the generated heat is dissipated to the outside of the resin-sealing body **31**.

As a result of practical experiments, it has been shown that the structure having the coupling portions **30** for coupling the common leads **24**M and the like can achieve a twofold or more improvement in a heat dissipation effect, as compared to conventional structures not having the coupling portion **30**.

Next, the description is given with reference to FIGS. **5**A to **7** with regard to a hybrid integrated circuit device according to a second embodiment of the present invention. FIG. **5**A is a cross-sectional view explaining a hybrid integrated circuit board according to this embodiment. FIG. **5**B is a plan view explaining the hybrid integrated circuit board according to this embodiment.

As shown in FIG. **5**A, a board having excellent heat dissipation characteristics is adopted as a hybrid integrated circuit board **41**, taking into account the heat generated by a semiconductor element and the like mounted on the board **41**. In this embodiment, the description is given with regard to the case in which an aluminum (hereinafter referred to simply as "Al") board **41** is used. Although the Al board is used as the board **41** in this embodiment, the board is not necessarily limited to this.

For example, a printed board, a ceramic board, a metal board, or the like may be used as the board **41** to implement this embodiment. A board made of copper (Cu), iron (Fe), an iron-nickel alloy (Fe—Ni), aluminum nitride (AlN), or the like may be used as the metal board.

The board **41** has an anodized surface, and the overall anodized surface is coated with insulating resin **42** having excellent insulating characteristics such as epoxy resin.

A conductive path **43***a* made of copper foil is formed on the insulating resin **42**. An active element **45** such as a power transistor, a small signal transistor, or an IC (integrated circuit), and a passive element **46** such as a chip resistor or a chip capacitor are mounted on the conductive path **43***a* with conductive material such as brazing material (e.g., solder or the like) **50**. The active element **45** and the like may be electrically connected to the conductive path **43***a* with silver (Ag) paste or the like. In the case of face-up mounting of the active element **45** such as the IC, electrodes of the IC and the like are bonded to the conductive path **43***a* through fine metal wires **47**. An outer lead **49** made of conductive material such as Cu or Fe—Ni is connected to an external

connect terminal **48** placed on the outer periphery of the board **41** with the brazing material (e.g., solder or the like) **50** or the like.

As shown in FIG. **5**B, the conductive path **43***a* is formed on the board **41**.

Moreover, the outer leads **49** are coupled by a tie bar **44** near the board **41** so that the tie bar **44** prevents resin from leaking when resin molding is performed. A part of the outer leads **49** have a coupling portion **54** between the tie bar **44** and the ends of the outer leads **49**, and are thus used as common leads **55**A, **55**B, **55**C, and **55**D. Since the common leads **55**A and the like are coupled by the coupling portion **54**, the common leads **55**A and the like have a common potential (i.e., a ground potential) as viewed in terms of electric potential.

Next, FIG. **6**A is a cross-sectional view explaining the hybrid integrated circuit device according to this embodiment. FIG. **6**B is a plan view explaining the hybrid integrated circuit device according to this embodiment.

As shown in FIG. **6**A, the overall surface of the board **41** is coated with the insulating resin **42**, and thereafter a complicated circuit is formed on the insulating resin **42**, and the outer lead **49** is bonded to the board **41** through the external connect terminal **48**. Then, by transfer molding with thermosetting resin, a resin-sealing body **51** is formed. The thermosetting resin has low viscosity and also has a lower curing temperature than the melting point (e.g., 183 degrees centigrade) of the brazing material (e.g., solder or the like) **50**. Thus, the inflow of the thermosetting resin while transfer molding does not cause falling-down, breaking, or bending of a fine Al wire having a diameter of about 40 μm, for example.

Moreover, in this embodiment, a die-cut surface **56** of the board **41** is located on the side of a rear surface **57** of the resin-sealing body **51**. In other words, the conductive path **43***a* and the like are formed on a surface **58** of the board **41** which is opposite to the die-cut surface **56** of the board **41**. A curved surface **59** is formed on the die-cut surface **56** of the board **41** while die-cutting the board **41**. While transfer molding, filling of resin is performed from a bottom surface of the board **41**. In this case, the curved surface **59** of the board **41** is utilized for smooth filling of the resin.

As shown in FIG. **6**B, holes **52** are formed in an outer periphery **53** of the board **41** (see FIG. **5**B), that is, a region of the board **41** on which the circuit and the like are not formed. Since the holes **52** are formed in the region belonging to both the outer periphery **53** of the board **41** and the insulating resin **42**, the structure has no problem in quality and moisture resistance. Moreover, the outer periphery **53** is provided in order to ensure a distance from a circuit region when pressing each board **41** separately. After all, the outer periphery **53** is dead space, which is effectively used as a contact region for pins to fix the board **41** while transfer molding.

Moreover, in this embodiment, the board having excellent thermal conductivity is used as the board **41**, so that the overall board **41** can be utilized as a heat sink, which can prevent temperatures of elements mounted on the board **41** from rising by the heat. Moreover, generated heat can be dissipated to the outside of the resin-sealing body **51** through the board **41**. Therefore, this embodiment includes the metal board **41** directly molded, so that superior heat dissipation characteristics can be achieved and thus circuit characteristics can be improved, as compared to the semiconductor device using the lead frame.

Next, FIG. **7** is a perspective view explaining the hybrid integrated circuit device according to this embodiment.

As shown in FIG. **7**, the outer leads **49** projecting out from one side of the resin-sealing body **51** are each curved and formed into a gull-wing shape. In this case, the common leads **55**A and the like are also formed into the gull-wing shape, and the coupling portion **54** is located in the vertical portions of the common leads **55**A and the like. Then, the outer leads **49** are bonded to corresponding conductive patterns on a printed wiring board with brazing material (e.g., solder or the like), as shown in FIG. **4** of the first embodiment.

As in the case of the first embodiment described above, the brazing material (e.g., solder or the like) **50** adheres to space between the common leads **55**A and the like with the coupling portion **54** therebetween, so that the common leads **55**A and the like are bridged with the brazing material (e.g., solder or the like) **50**. This is accomplished by utilizing the surface tension of the brazing material (e.g., solder or the like) **50**. The space between the common leads **55**A and the like is filled with the brazing material (e.g., solder or the like) **50**, so that the common leads **55**A and the like function as a large lead.

With this structure, the common leads **55**A and the like of the outer leads **49** each have a large surface area and a great thickness. Thus, the heat generated by the active element **45** or the passive element **46** is transferred from the board **41** to the common leads **55**A and the like bridged with the brazing material (e.g., solder or the like) **50**. Then, the generated heat is dissipated to the outside of the resin-sealing body **51**.

Note that, in the second embodiment, the description has been given with regard to the case in which the outer leads extend from one side of the board. However, the preferred embodiment of the present invention is not limited to this case. For example, the outer leads may extend from opposite sides of the board. In this case, the above-mentioned heat dissipation characteristics also can be improved. In addition, various modifications are possible within a range not departing from the gist of the invention.

The semiconductor device of the preferred embodiments includes the island having the integrated circuit chip mounted thereon, the common leads, the coupling portion, and the brazing material with which the common leads are bridged. The common leads, the coupling portion, and the brazing material enable efficient dissipation of the heat generated by the integrated circuit chip to the outside of the resin-sealing body. Thus, this structure can prevent the integrated circuit chip or the semiconductor device itself from being damaged by the heat.

Moreover, in the semiconductor device of the preferred embodiments, is obtained the effect that the brazing material used for bridging allows an increase in the widths of the common leads, even when a larger number of pins formed from the leads are adopted, or a larger number of pins are adopted in an extremely thin metal board. Moreover, the thicknesses of the common leads can be equivalently increased, so that heat dissipation characteristics can be improved.

Furthermore, in the semiconductor device of the preferred embodiments, the discrete leads and the common leads are each formed into the gull-wing shape, so that plenty of brazing material can adhere to the curved portions of the common leads. Thus, when the common leads are bonded to the conductive patterns with the brazing material, the surface tension of the brazing material can be utilized to realize the structure that facilitates bridging the common leads.

In the hybrid integrated circuit device of the preferred embodiments, the top surface of the metal board is coated with the insulating resin. The conductive pattern is formed

on the insulating resin surface, and the active element and the passive element are mounted on the conductive pattern. The resin-sealing body is formed so as to coat the pattern and the elements. The heat generated by the active element or the passive element can be dissipated through not only the metal board but also the outer leads projecting out from the resin-sealing body. The common leads are formed in the outer leads, thus, heat dissipation characteristics can be further improved.

What is claimed is:

1. A semiconductor device including:

an island on which a semiconductor element is mounted;

a plurality of discrete leads each having an end extending near the island;

a plurality of common leads coupled to the island; and

a resin-sealing body molding the semiconductor element, the island, the discrete leads, and the common leads,

wherein the common leads projecting out from the resin-sealing body are provided with a coupling portion.

2. The semiconductor device according to claim 1, wherein the common leads are bonded to a conductive pattern with a conductive adhesive, and the common leads are bridged with the conductive adhesive between the coupling portion and the conductive pattern.

3. The semiconductor device according to claim 1, wherein the common leads are coupled to both sides of the island.

4. The semiconductor device according to claim 1, wherein the common leads are each formed into a gull-wing shape.

5. A hybrid integrated circuit device including:

a conductive pattern formed at least on a surface of a hybrid integrated circuit board;

a semiconductor element or a passive element mounted on the conductive pattern;

a plurality of leads connected to the conductive pattern and extending outside, the leads acting as an output or an input; and

a resin-sealing body made of a thermosetting resin, which coats at least the surface of the board by transfer molding,

wherein the leads have a plurality of common leads projecting out from the resin-sealing body, and the common leads are coupled by a coupling portion.

6. The hybrid integrated circuit device according to claim 5, wherein the common leads are bonded to a conductive pattern with a conductive adhesive, and the common leads are bridged with the conductive adhesive between the coupling portion and the conductive pattern.

7. The hybrid integrated circuit device according to claim 5, wherein the common leads are each formed into a gull-wing shape.

8. The hybrid integrated circuit device according to claim 5, wherein the board is made of a metal board, and has a die-cut surface which is opposite to the surface of the board on which the conductive pattern is formed, and the die-cut surface is located on a side of a rear surface of the resin-sealing body.

9. The semiconductor device according to claim 1, wherein the coupling portion is formed between a side surface of the resin-sealing body and ends of the common leads.

10. The semiconductor device according to claim 4, wherein the coupling portion is formed on a vertical portion of the gull-wing shape.

11. The hybrid integrated circuit device according to claim 5, wherein the coupling portion is formed between a side surface of the resin-sealing body and ends of the common leads.

12. The hybrid integrated circuit device according to claim 7, wherein the coupling portion is formed on a vertical portion of the gull-wing shape.

* * * * *

EXHIBIT 4

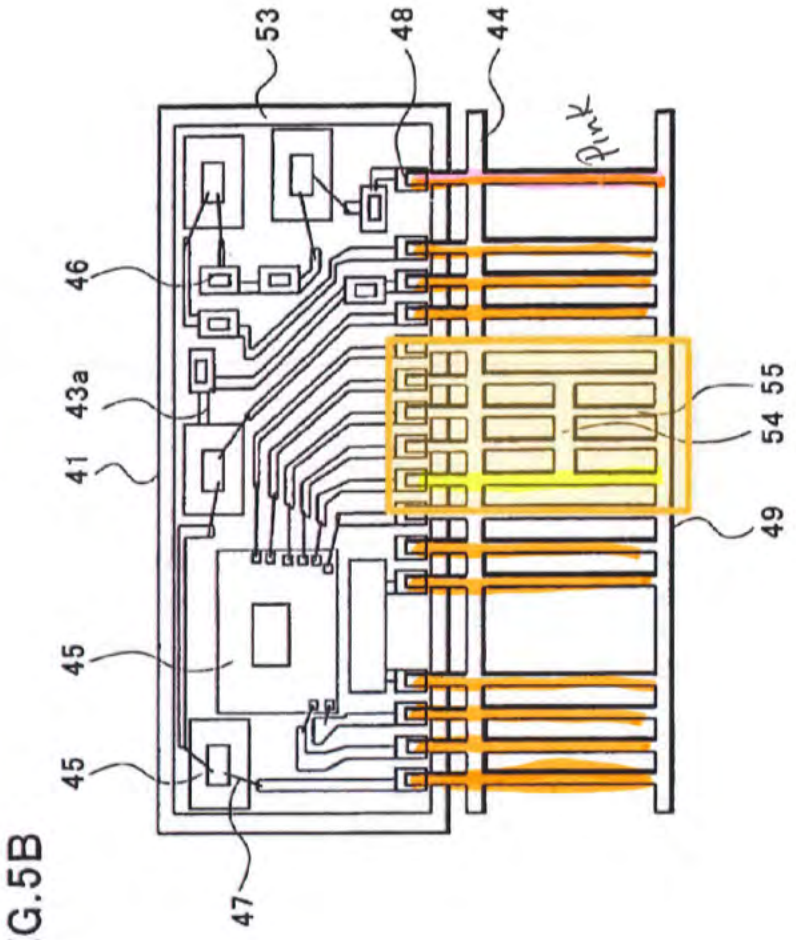
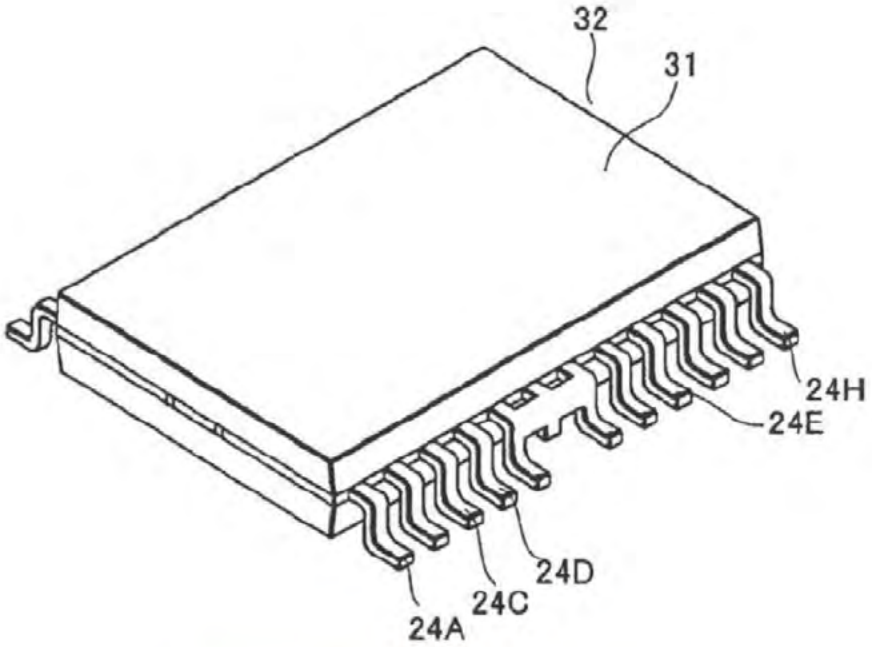
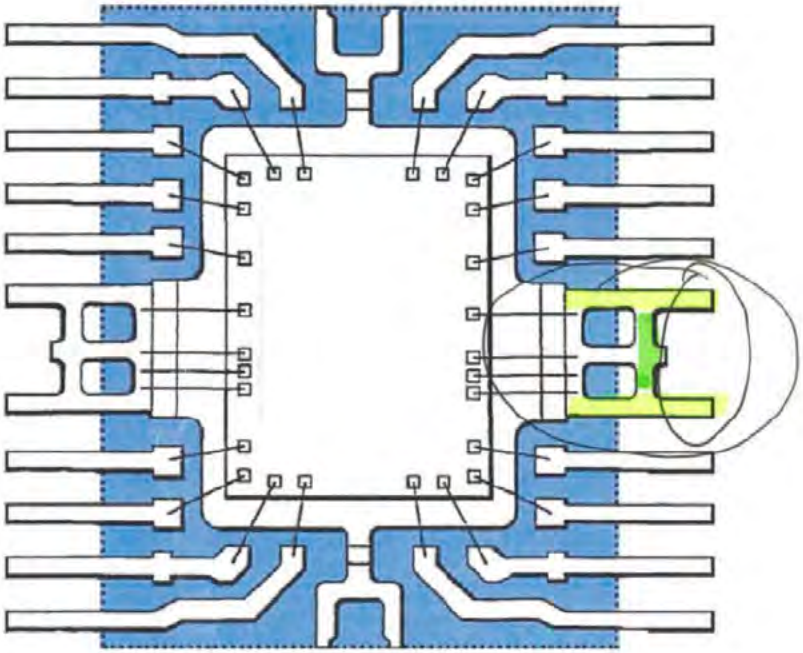


FIG.5B

'211 Figure 5B

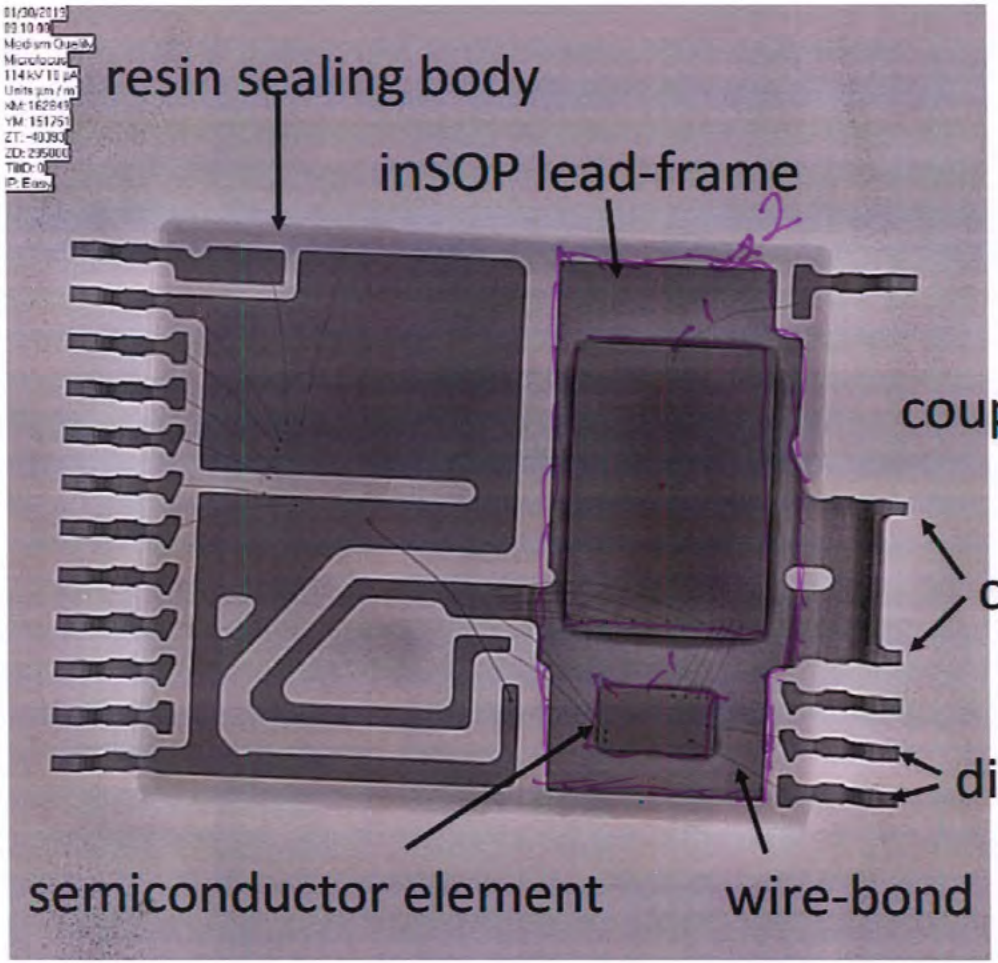
EXHIBIT 5


32
31
24H
24E
24D
24C
24A




DEPOSITION
EXHIBIT
23

EXHIBIT 6



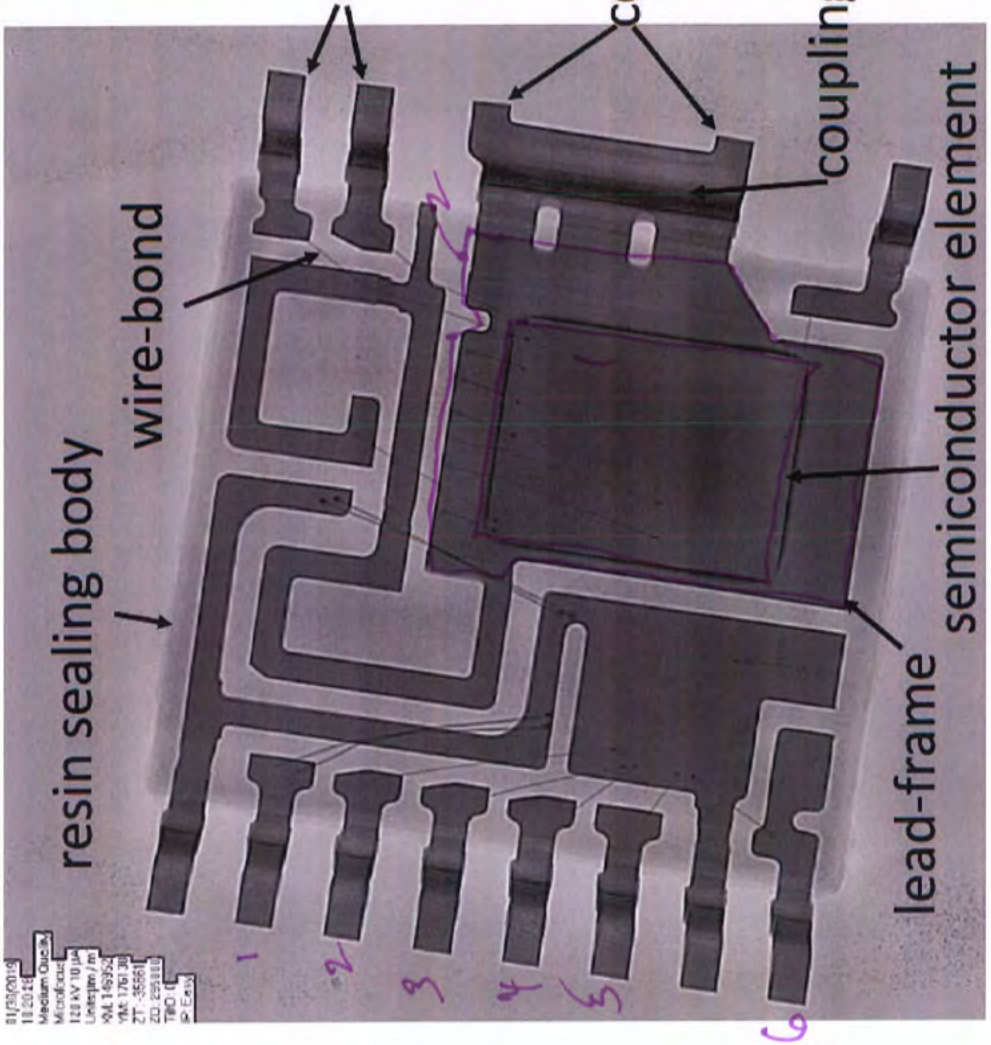

discrete leads
common leads
coupling portion
resin sealing body
wire-bond
lead-frame
semiconductor element

EXHIBIT 7

(19) **Japan Patent Office** (JP)

(11) Japanese Unexamined Patent Application Publication Number

(12) **Japanese Unexamined Patent Application Publication** (A)

61-53752

(51) Int. Cl.[4]	Identification codes	JPO file numbers	(43) Publication date March 17, 1986
H 01 L 23/48		7357-5F	

Request for examination Not yet requested Number of inventions 1 (Total of 5 pages)

(54) Title of the invention	LEAD FRAME	
	(21) Japanese Patent Application	S59-174957
	(22) Date of Application	August 24, 1984
(72) Inventor	Kazuo Shimizu	Hitachi Ltd., Kozawa Plant 111 Nishiyokotemachi, Takazaki-shi
(72) Inventor	Kazuo Hoya	Hitachi Ltd., Kozawa Plant 111 Nishiyokotemachi, Takazaki-shi
(71) Applicant	Hitachi Ltd.	4-6 Kandasurugadai, Chiyoda-ku, Tokyo
(74) Agent	Patent attorney Teruo Takahashi	and 1 other

SPECIFICATION

TITLE OF THE INVENTION

Lead Frame

SCOPE OF PATENT CLAIMS

1. A lead frame in which a tab for mounting a pellet is supported by a tab-suspending lead on a pair of lead frame outer frames, said lead frame characterized by connecting a cooling fin between the tab-suspending lead and the tab.

DETAILED DESCRIPTION OF THE INVENTION

(TECHNICAL FIELD)

The present invention relates to a technology that is particularly effective when used in lead frames for semiconductor devices.

(PRIOR ART)

As is indicated in Solid State Technology/Japan Edition, September 1982, pp. 69-77, advances are occurring in semiconductor devices, particularly in regard to providing increased functionality and decreased size in IC package units. An example thereof is the desire for the development of power ICs having high-output circuits for motor drives.

However, by providing a high-output circuit, the heat that is generated due to high power consumption by the circuit has a detrimental influence on the operation of other circuits. For this reason, it is necessary for this heat to escape from the package. In the past, a heat sink along with corresponding heat-dissipating fins have been separately provided in an isolated state for each package. Consequently, heat transfer efficiency from the tabs carrying the pellets to the heat sinks has been poor, package thermal resistance has increased, and obtaining a high power IC package has been difficult. In addition, it has not been possible to avoid costly large-format configurations.

(OBJECT OF THE INVENTION)

An object of the present invention is to improve heat conduction properties from tabs to heat dissipating fins by integrating the heat dissipating fins with the tabs that support the pellets, and to provide a lead frame for a semiconductor device that manifests high-output functionality, in spite of being a small multi-pin IC package.

Other objects of the present invention as well as novel defining characteristics will become clear from the description of the specification and the attached drawings.

(SUMMARY OF THE INVENTION)

The following is a simple description of a summary of a typical device of the present invention disclosed in this application.

Specifically, in the present invention, by integrating and connecting broad heat dissipating fins between the tabs and the tab-suspending leads, the heat in the tabs that have been heated by the pellet is rapidly absorbed by the heat dissipating fins and the pellet on the tabs is effectively cooled. By this means, a small high-power semiconductor device can be obtained inexpensively.

(EXAMPLES OF EMBODIMENT)

Fig. 1 is a partial sectional view of an example of embodiment of the lead frame of the present invention. In this example of embodiment, a lead frame is presented that is used in a mini square package. This figure shows only one lead frame pair part, which also may be formed, e.g., by connecting seven packages lengthwise. Lead positioning holes **2** are provided at a constant spacing on the outer frame **1** of the lead frame. In addition, a pellet having integrated heat dissipating fins **4** and a tab **5** for mounting is connected via tab-suspending leads **3** on the pair of lead frame outer frames **1**. For this reason, with this frame, the number of pins can be increased by two more than when the tab-suspending leads are provided in isolation. A mold line is shown in this figure, represented by a line broken with a single dot. The heat-dissipating fin **4** is divided into three by passage holes **6** for resin loading in the vicinity of the mold line. One is the tab-suspending lead, and the other two are larger than the outer lead **9** inside the dam tie-bar **7**, but have the same shape as the outer leads outside the dam tie-bar **7**. The reasons for this relate to considerations regarding mountability to the printed substrate and heat dissipation properties, as described below.

In addition, the dam tie-bar **7** is connected to the pair of heat dissipating fins **4** so as to surround the tab **5** while providing a constant spacing, and multiple inner leads **8** and outer leads **9** are connected to the dam tie-bar **7**. In addition, the heat dissipation properties and thermal conductivity are made more efficient by making the base ends of the heat dissipating fins **4** much wider than the inner leads **8** and making them wider towards their ends.

Au wires or the like are wire-bonded to the pad part of the pellet at the end of each inner lead **8**.

10 is a positioning hole for the tab 5 of the pellet.

When the pellet is configured as a high-power IC using this lead frame shape, the heat that is generated can be conveyed through the tab **5** to the heat-dissipating fins **4**, the exposed portions in the heat-dissipating fins **4** can be additionally cooled from the resin package main body by external air, and the heat dissipating fins **4** can be indirectly cooled through contact on another heat sink.

In addition, after the pellet is placed on the tab **5**, wire bonding is carried out, the lead frame is held between the upper metal mold and lower metal mold, resin is injected at 20 to 100 kg/cm^2, and curing is allowed to occur. The semiconductor device package shown in Fig. 2 and Fig. 2b is then obtained by cutting away the dam tie-bars **7** and the tab leads **3** as desired.

Fig. 2 shows the mounting condition on a printed substrate **20** (wiring not shown.)

It should be noted in the drawings that the shape of the package and the layout of the outer leads **9** and a part **9'** of the heat-dissipating fins are similar to that of mini square packages, or differ only somewhat at the tab-suspending leads **3**. Specifically, mini square package production and mounting equipment can be used without modification. The lead frame described above also is similar to lead frames used for mini square packages in portions other than the heat-dissipating fins, and so pellet attachment devices and wire bonders can be used together.

If there are no passage holes **6** for resin loading, the surface area of the heat dissipating fins **4** will be great, the resin bonding forces above and below will be weak at this location, and there will be a tendency for water ingress. In this example of embodiment, passage holes **6** are provided, and the interiors of the passage holes **6** are filled with resin, thereby improving binding between the heat dissipating fins **4** and the resin and preventing ingress of water.

In addition, when the dam tie-bars **7** or tab-suspending leads **3** are cut away, the cutting parts **A** of the tab-suspending leads **3** are cut off inside the distal end parts **B** of the outer leads **9**, thereby preventing protrusion of the distal ends of the tab-suspending leads **3** past the distal end parts of the outer leads **9**.

When mounting onto a printed substrate, mounting can be done in holes **21** formed in the pattern in the same manner as with electrode patterns for normal mini square packages. Specifically, the electrode pattern can be standardized, and design of printed substrates is facilitated.

In this manner, with semiconductor packages having the lead frame of the present invention, operation with a power consumption (Pd) of about 1.5 to 2 W is possible, even when a substrate is used that has a thickness of 0.25 mm and copper-based metal as the fame material. In addition, the tab-suspending leads **3** constitute some of the heat dissipating parts along with the heat dissipating fins, and effective use of the tab suspending leads **3** is thus achieved.

(EFFECT)

(1) The present invention has a configuration in which the lead frame outer frames and the tabs are connected by heat dissipating fins via tab-suspending leads. Therefore, multiple pins can be used, and the heat that has been generated by the pellet can be directly transferred to the heat dissipating fins having low thermal resistance. This heat also can be dissipated into external air via the tab-suspending leads that border the outside of the package. Pellet heat dissipation is therefore made efficient, and production of a small semiconductor device with high power consumption is possible.

(2) The present invention allows heat from the tabs to be rapidly absorbed by the heat dissipating fins, because the heat dissipating fins are substantially greater in unit surface area than the inner leads, and the heat dissipation efficiency of the pellet referred to in (1) above therefore can be increased.

(3) The present invention has increased resin (mold material) density relative to the heat dissipating fins, because resin filling passage holes are provided in the heat dissipating fins, which can effectively prevent ingress of water and mechanical damage to the package interior.

The present invention has been described in detail by the inventors of the present invention based on examples of embodiment, but the present invention is not restricted to these examples of embodiments, and various modifications are possible within a scope that is defined by the gist thereof.

(FIELD OF USE)

Although the inventors of the present invention, in the background of present invention described above, have described use of the present invention in mini square package technology, the field of use is not restricted thereto, and the invention may be used in other packages, such as dual in-line packages.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view of a partial sectional view of an example of embodiment of the lead frame of the present invention.

Fig. 2a and Fig. 2b are perspective views of the semiconductor package.

1 Lead frame outer frame
3 Tab-suspending lead
4 Cooling fin
5 Tab
6 Resin loading passage hole
7 Dam tie-bar
8 Inner lead
9 Outer lead

Agent: Patent attorney Teruo Takahashi
[seal: illegible]

Fig. 1

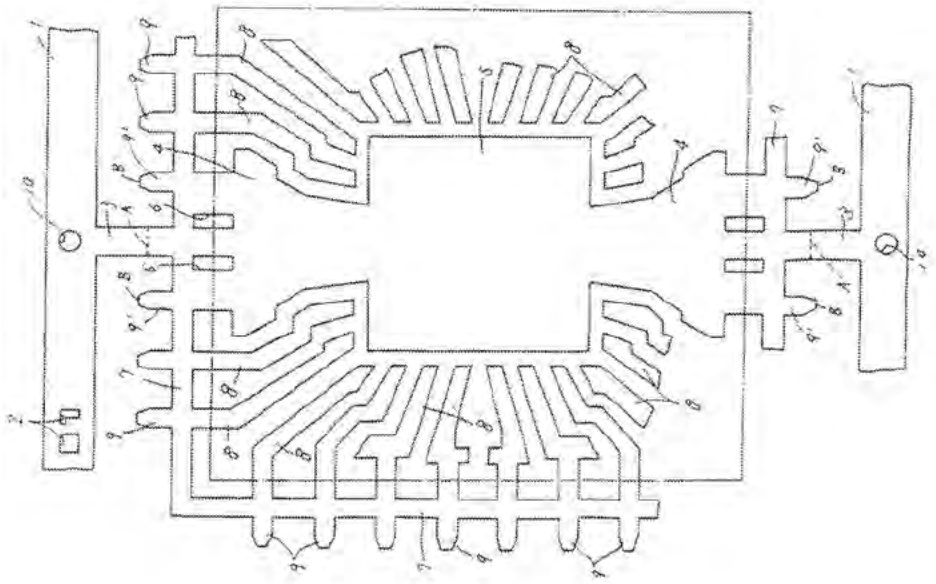


Fig. 2a

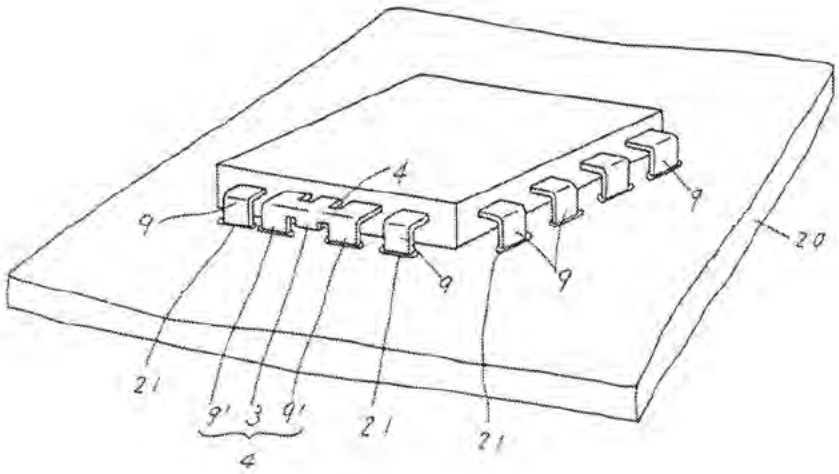
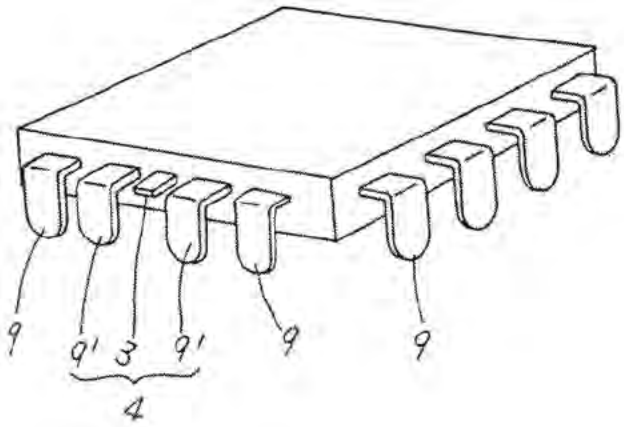


Fig. 2b



TRANSPERFECT

I attest that the attached document is a true and accurate translation of JPS6153752A.

I performed the proofreading and am fluent in English and Japanese.

I understand that wilful false statements and the like are punishable by fine or imprisonment or both. These statements are true and are made of my own knowledge.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on 29 December 2017 at Bethesda, MD USA.

Signed

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－53752

⑤1Int.Cl.⁴　識別記号　庁内整理番号　⑬公開　昭和61年(1986)3月17日
H 01 L 23/48　7357－5F

審査請求　未請求　発明の数 1　（全5頁）

⑭発明の名称　リードフレーム

⑳特　願　昭59－174957
㉒出　願　昭59(1984)8月24日

㉒発明者　清水　一男　高崎市西横手町111番地　株式会社日立製作所高崎工場内
㉒発明者　保谷　和男　高崎市西横手町111番地　株式会社日立製作所高崎工場内
㉑出願人　株式会社日立製作所　東京都千代田区神田駿河台4丁目6番地
㉔代理人　弁理士　高橋　明夫　外1名

明　細　書

発明の名称　リードフレーム

特許請求の範囲

1．一対のリードフレーム外枠にタブつりリードによってペレット搭載用のタブを支持させたリードフレームであって、上記タブつりリードとタブとの間に冷却フインを連設したリードフレーム。

発明の詳細な説明

〔技術分野〕

本発明は半導体装置のリードフレームに適用して特に効果のある技術に関する。

〔背景技術〕

日本エス．エス．ティ株式会社発行、「Solid State technology／日本版」，1982年9月発行　p59～p77にも示されるように半導体装置、特に、ICパッケージ単位ごとの多機能化，小形化が進んでいる。その中で、例えばモータ駆動のための高出力回路を設けたパワーICの出現が望まれている。

しかしながら、高出力回路を設けることによって、大きな回路損失に伴って発生した熱が他の回路の動作を阻害する。このため、その熱をパッケージ外に逃がす必要があり、従来は、放熱フィンに相当するヒートシンクを、パッケージごとに独立分離した状態で設けていた。したがって、ペレットを載せたタブからヒートシンクへの熱伝導効率が悪く、パッケージの熱抵抗が大きくなり、高出力タイプのICパッケージを得ることが難しいことがわかった。また、構成の大型化，高価格を免れ得なかった。

〔発明の目的〕

本発明の目的は、ペレットを載せるタブに放熱フィンを一体化する様にしてタブから放熱フィンへの熱伝導性を改善し、ICパッケージが小形かつ多ピン形であるにも拘わらず、高出力機能を具現する半導体装置のリードフレームを提供することにある。

本発明の前記ならびにそのほかの目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

〔発明の概要〕

本願において開示される発明のうち代表的なものの概要を簡単に述べると、下記の通りである。

すなわち、本発明はタブとタブつりリードとの間に幅広の放熱フィンを一体連設することによって、ペレットにより熱せられるタブの熱を放熱フィンに迅速に吸収させ、タブ上のペレットを効率的に冷却する。これにより、高パワーの半導体装置を小形かつ安価に得ることができる。

〔実施例〕

第1図は本発明のリードフレームの一実施例を一部破断して示してある。この実施例では、ミニ・スクウェア・パッケージ用のリードフレームについて示してある。同図においては、一対のリードフレーム部分だけ図示してあるが、例えばパッケージ7個分の長さに連続して形成されている。このリードフレーム外枠1にはリード位置決め孔2が一定の間隔で設けられている。また、一対のリードフレーム外枠1にはタブつりリード3を介して放熱フィン4を一体に有するペレット，載置用ペレットのタブ5に対する位置決め孔である。

かかるリードフレーム形状では、ペレットがハイパワーICとして構成された場合に生じる熱をタブ5を通じて放熱フィン4に伝達でき、この放熱フィン4のうち、レジンパッケージ本体から露出した部分を外気にさらして空冷したり、この放熱フィン4を他のヒートシンク上に接触させて間接冷却したりすることができる。

また、上記タブ5上にはペレットが設置され、上記ワイヤボンドを行った後、リードフレームが上金型，下金型の間に挟持され、20～100 Kg/cm² でレジンを注入して硬化させ、さらにダムタイバ7やタブリード3を所望に切除し、第2の図、第2b図に示す半導体装置のパッケージを得る。

第2の図はプリント基板20（配線は図示せず）に実装した状態を示す。

同図において注目すべきは、パッケージ形状及びアウターリード9と放熱フィンの1部9'の配列がミニ・スクウェア・パッケージと同等又はタブタブ5が連設されている。このためこのフレームで独立してタブつりリードを設けた場合より、2本ピンを多くできる。同図に一点鎖線で示されるのは、モールドラインを示している。この放熱フィン4はモールドライン付近でレジン充填用透孔6により3つにわかれている。1つはタブつりリードとなり、他の2つはダムタイバ7内ではアウタリード9より太く、ダムタイバ7外ではアウタリード形状と同一の形状をとっている。この理由は、後述するようにプリント基板への実装性，放熱性等を考慮したことによる。

また、一対の放熱フィン4には、タブ5を一定距離隔てて囲む様にダムタイバ7が連設され、このダムタイバ7に多数のインナリード8およびアウタリード9が連設されている。さらに、放熱フィン4の基部はインナリード8よりも十分に広く、しかも末広がりになって放熱性，熱伝導性を効率化している。

なお、各インナリード8端にはペレットのパッド部にAu線などがワイヤボンドされる。10は

つりリード3部で多少異なっているだけであるということである。すなわち、ミニ・スクウェア・パッケージの生産及び実装設備をそのまま使用することができる。前述のリードフレームにおいてもミニ・スクウェア・パッケージに使用するリードフレームと放熱フィン以外の部分は同一としているため、ペレット付け装置，ワイヤーボンダを共用して使用することができる。

レジン充填用透孔6がない場合、放熱フィン4の面積が大で、この部位での上下のレジンの結着力が劣るほか、水の侵入に対して弱い。この実施例では透孔6を設けることにより、この透孔6内にレジンを充てんすることにより、放熱フィン4とレジンとの密着性を改善し、水の侵入を防止している。

また、ダムタイバ7やタブつりリード3を切除する場合に、タブつりリード3の切断部Aをアウタリード9の先端部Bより内側で切り落すことにより、アウタリード9先端部よりタブつりリード3先端が突出するのを防ぐことができプリント基

板に実装する場合に通常のミニ・スクウェア・パッケージの電極パターンと同じパターンで形成された穴21に実装することができる。すなわち、電極パターンの規格化が可能となり、プリント基板の設計が容易になる。

この様に、本発明のリードフレームを有する半導体パッケージでは、フレーム材料に銅系金属の厚み0.25㎜の板体を使った場合でも、消費電力（Pd）が略1.5W～2Wでの作動が可能になった。また、タブつりリード3は放熱フィンとともに放熱部の一部を構成し、タブつりリード3の有効利用を図ることができる。

〔効　果〕

(1)　本発明はリードフレーム外枠とタブとをタブつりリードを介して放熱フィンにより連結した構成としたことにより、多ピン化できるとともにペレットで発生した熱を熱抵抗の小さい放熱フィン直接伝達することができ、この熱をさらにパッケージ外に臨ませられるタブつりリードを介して外気に放熱できる。従って、ペレットの放熱が効率化し、小形大消費電力の半導体装置の製作が可能になる。

(2)　本発明は放熱フィンをインナリードよりも単位面積を十分に広くとることによって、タブの熱を迅速に放熱フィンに吸収させることができ、上記(1)のペレットの放熱効率を著るしく高めることができる。

(3)　本発明は放熱フィンにレジン充てん用透孔を設けることによって、放熱フィンに対するレジン（モールド材）の密着性を高め、パッケージ内への水の侵入、機械的破損を有効に防止できる。

以上、本発明者によってなされた発明を実施例にもとづき具体的に説明したが、本発明は上記実施例に限定されるものでなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

〔利用分野〕

以上の説明では主として本発明者によってなされた発明をその背景となった利用分野であるミニ・スクウェア・パッケージ技術に適用した場合について説明したが、それに限定されるものでなく、他のパッケージ例えばデュアルインラインのパッケージに適用できる。

図面の簡単な説明

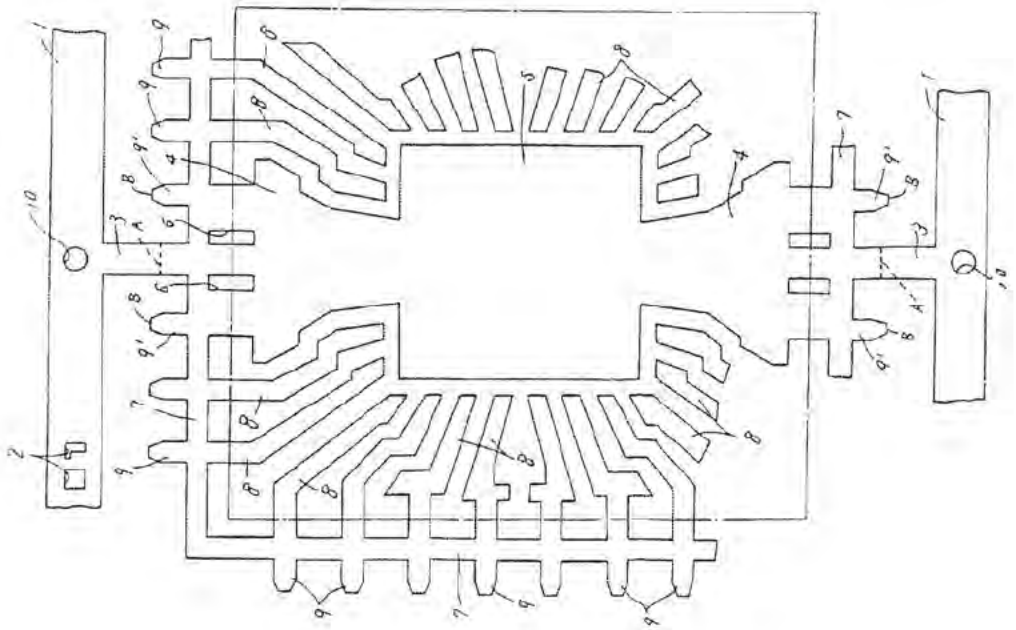
第1図は本発明のリードフレームの一実施例を示す一部破断した平面図。

第2(α)図、第2b図は半導体パッケージの斜視図である。

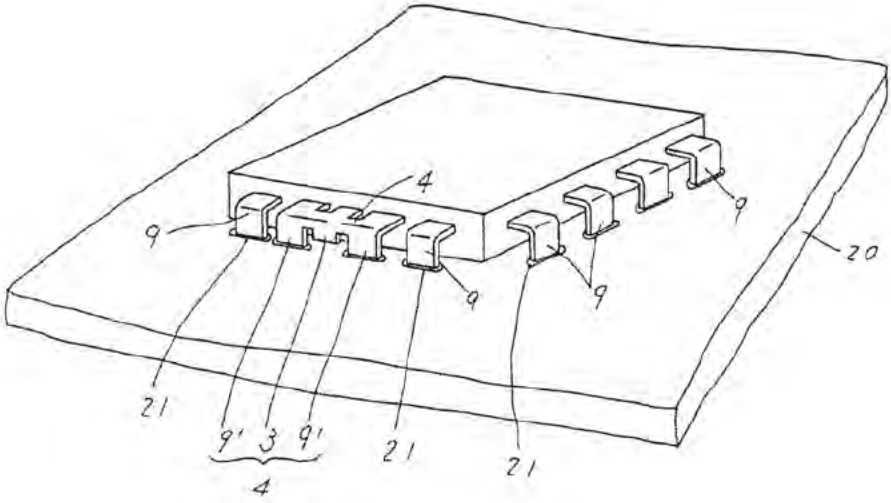
1…リードフレーム外枠、3…タブつりリード、4…放熱フィン、5…タブ、6…レジン充填用透孔、7…ダムタイバ、8…インナリード、9…アウタリード。

代理人　弁理士　　高　橋　明　夫

第 1 図



第 2 a 図



第 2 b 図

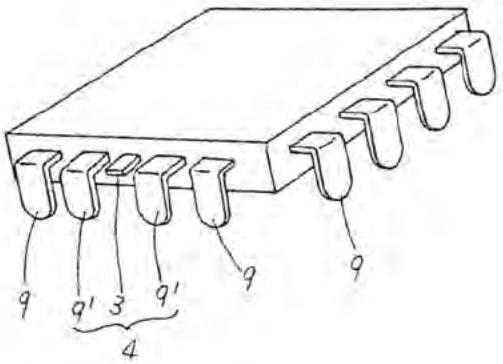


EXHIBIT 8

(19) **Japan Patent Office** (JP)

(11) Japanese Unexamined Patent Application Publication Number

(12) **Japanese Unexamined Patent Application Publication** (A)

62-45054

(51) Int. Cl.[4]	Identification codes	JPO file numbers	(43) Publication date February 27, 1987
H 01 L 23/48		7735-5F	

Request for examination Not yet requested Number of inventions 1 (Total of 2 pages)

(54) Title of the invention	SEMICONDUCTOR DEVICE	
	(21) Japanese Patent Application	S60-184722
	(22) Date of Application	August 21, 1985
(72) Inventor	Hitoshi Hoshino	NEC Corp. 5-33-1 Shiba, Minato-ku, Tokyo
(71) Applicant	NEC Corp.	5-33-1 Shiba, Minato-ku, Tokyo
(74) Agent	Patent attorney Susumu Uchihara	

SPECIFICATION

1. TITLE OF THE INVENTION

Semiconductor Device

2. SCOPE OF PATENT CLAIMS

A resin-sealed type semiconductor device having a sealed resin body and a plurality of external leads that lead out externally from this sealed resin body, said semiconductor device characterized by a plurality of adjacent external leads being bonded.

3. DETAILED DESCRIPTION OF THE INVENTION

[INDUSTRIAL USE FIELD]

The present invention relates to a resin-sealed type semiconductor integrated circuit, and specifically relates to decreasing the thermal resistance of a package thereof.

[PRIOR ART]

Fig. 3a is a side view of a conventional DIP package resin-sealed integrated circuit, and Fig. 3(b) is a plan view of a conventional flat package resin-sealed integrated circuit. In these figures, outer leads **2** and **5** respectively lead out from the side faces of the sealed resin bodies **1** and **4**.

(PROBLEMS TO BE SOLVED BY THE INVENTION)

Regarding dissipation of heat in the above type of conventional resin-sealed integrated circuits, some diffuses directly to an external part from the surface of the sealed resin body **1**, and some is transmitted through the outer leads and diffuses to the substrate with attached leads. However, when heat dissipation characteristics are to be improved, a means has been adopted whereby the thermal resistance of the sealing resin is decreased. However, providing the sealing resin with low thermal resistance leads to problems with moisture resistance and temperature cycling, and there is the disadvantage that resolving these problems increases costs due to a large increase in development expenditures.

(MEANS FOR SOLVING THE PROBLEMS)

In the present invention, as a response to the problems described above, at least two adjacent external leads that lead off from the sealed resin body are bonded, thereby increasing heat diffusion across the external leads.

(EXAMPLES OF EMBODIMENT)

The present invention is described below using examples of embodiment

Fig. 1 is a side view of an example of embodiment of the present invention. In the figure, of the external leads **2**, **2**, . . . that lead out externally from the side face of a DIP package sealed resin body **1** and also bend downwards, a group of adjacent external leads is integrally bonded with a connecting part **3**, and the remainder of the external leads **2**, **2** remain separate from each other without modification.

Fig. 2 is a plan view of another example of embodiment of the present invention. In the figure, of the plurality of external leads **5**, **5**, . . . that lead out in four directions from the side faces of the flat package sealed resin body **4**, a group of two adjacent external leads on the left side face are bonded by a bonding part **6**, and a group of three adjacent external leads on the bottom side face are integrally bonded by a bonding part 7.

(EFFECT OF THE INVENTION)

As described above, in the present invention, a plurality of external leads are bonded to increase the heat dissipating surface area, thereby having the effect of providing the resin sealed package with low thermal resistance. In addition, by changing the combinations of bonded external leads, effects can be expected whereby the positions of the external leads can be specified.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side view of an example of embodiment of the present invention. Fig. 2 is a plan view of another example of embodiment of the present invention. Fig. 3a is a side view of an example of a conventional resin-sealed integrated circuit. Fig. 3b is a plan view of another example.

1, 4 Sealed resin body
2, 5 External leads
3, 6 Bonding part for two external leads
7 Bonding part for three external leads

Agent: Patent attorney Susumu Uchihara
[seal: illegible]

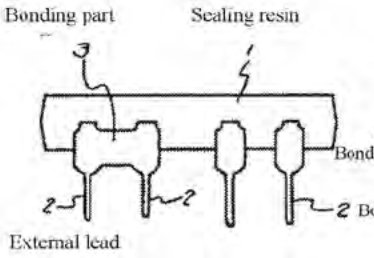


Fig. 1

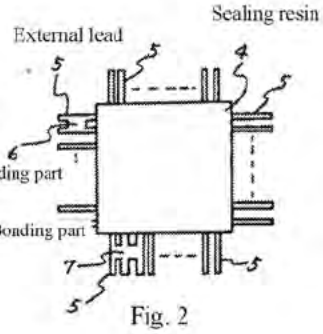


Fig. 2

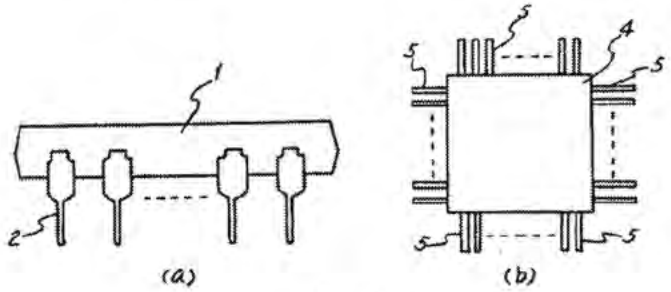


Fig. 3

TRANSPERFECT

I attest that the attached document is a true and accurate translation of JPS6245054A.

I performed the proofreading and am fluent in English and Japanese.

I understand that wilful false statements and the like are punishable by fine or imprisonment or both. These statements are true and are made of my own knowledge.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on 27 December 2017 at Bethesda, MD USA.

Signed

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭62－45054

⑤1Int.Cl.⁴	識別記号	庁内整理番号	㊸公開　昭和62年(1987)2月27日
H 01 L 23/48		7735－5F	

審査請求　未請求　発明の数 1　（全2頁）

⑤4発明の名称　半導体装置

㉑特　願　昭60－184722

㉒出　願　昭60(1985)8月21日

㉒発明者　星野　仁　東京都港区芝5丁目33番1号　日本電気株式会社内

㉑出願人　日本電気株式会社　東京都港区芝5丁目33番1号

㉔代理人　弁理士　内原　晋

明　細　書

1. 発明の名称

半導体装置

2. 特許請求の範囲

封止樹脂体と、この封止樹脂体から外部に引出された多数の外部リードを有する樹脂封止型の半導体装置において、前記隣接する複数の外部リードが結合されていることを特徴とする半導体装置。

3. 発明の詳細な説明

〔産業上の利用分野〕

本発明は樹脂封止型半導体集積回路に関し、特にそのパッケージの低熱抵抗化に関するものである。

〔従来の技術〕

第3図(a)は従来のＤＩＰパッケージの樹脂封止型集積回路の側面図、同図(b)は従来のフラットパッケージの樹脂封止型集積回路の平面図である。これらの図において、封止樹脂体1および4の側面からそれぞれ外部リード2および5が個々に引出されている。

〔発明が解決しようとする問題点〕

上記のような従来の樹脂封止型集積回路の放熱は、封止樹脂体1の表面から外部に直接放散する分と、外部リードを伝わって、リード取付け基板に放散される分とあるが、より放熱特性をよくしようとする場合、封止樹脂の熱抵抗を小さくする手段がとられていた。しかし、封止樹脂の低熱抵抗化は、耐湿性，温度サイクル性の問題を生じ、この問題を改善するには、開発費用の増大によりコスト高となる欠点がある。

〔問題点を解決するための手段〕

上記問題点に対し、本発明では、封止樹脂体から引き出されている外部リードの隣接するものの少くとも2本を結合させて、外部リードを伝わっての熱放散を大きくしている。

〔実施例〕

つぎに本発明を実施例により説明する。

第１図は本発明の一実施例の側面図である。図において、ＤＩＰパッケージの封止樹脂体１の側面から外部に引出され、さらに下方に曲げられている外部リードの２，２，……のうち、隣り合う一組の外部リードは、連結部３により一体に結合され、残りの外部リード２，２はそのまま個々に独立している。

第２図は本発明の他の実施例の平面図であり、図において、フラットパッケージの封止樹脂体４の側面から４方に引出されている多数の外部リード５，５，……のうち、左側面の隣り合う２本一組の外部リードは結合部６により結合され、さらに下側面の隣り合う一組３本の外部リードが結合部７により一体に結合されている。

〔発明の効果〕

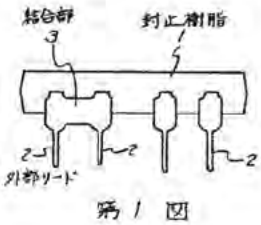
以上説明したように本発明は、複数の外部リードを結合し、放熱面積を大きくすることにより、樹脂封止パッケージの低熱抵抗化をできる効果がある。また、結合する外部リードの組合せを変えることにより、外部リードの位置を明確に出来る効果が期待出来る。

4. 図面の簡単な説明

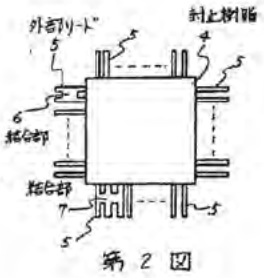
第１図は本発明の一実施例の側面図、第２図は本発明の他の実施例の平面図、第３図(a)は従来の樹脂封止型集積回路の一例の側面図、同図(b)は他の例の平面図である。

１，４……封止樹脂体、２，５……外部リード、３，６……２本の外部リード結合部、７……３本の外部リード結合部。

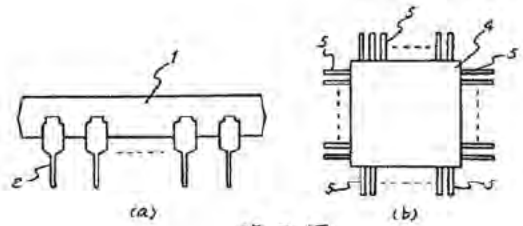
代理人　弁理士　内原　晋



第１図



第２図



第３図

EXHIBIT 9

Toyu Yazaki
6348 Meadowridge Drive,
Santa Rosa, CA 95409

Telephone: (415) 505-0581
FAX: (772) 619-0664
e-mail: toyuyyaz@gmail.com

I, Toyu Yazaki, hereby declare that I am a professional interpreter and translator, with over twenty-five (25) years of professional experience, and am knowledgeable of and well acquainted with the Japanese language and the English language.

The document in the English language attached hereto is to the best of my ability, knowledge and expertise the correct English translation of JPA_1987206868 written in the Japanese language.

I declare under penalty of perjury under the laws of United States that the foregoing is true and correct. Executed this 21st day of March 2018 at Santa Rosa, CA.

Toyu Yazaki

(19) Japan Patent Office (JP)

(12) **(UNEXAMINED) PATENT APPLICATION PUBLICATION (A)**

(11) Patent Application Publication Number: S62-206868
(43) Publication Date: September 11, 1987

(51) Int. Cl.[4]	Identification Symbol	Office file No.
H01L 23/48		7735-5F
23/34		A-6835-5F

Request for Examination: Not yet requested Number of inventions: 1
(Total of 5 pages)

---

(54) Title of the Invention: Electronic device

(21) Patent Application No.: S61-48398
(22) Application Date: March 7, 1986

(72) Inventor: Shigeo Otaka
c/o Takasaki Works, Hitachi, Ltd.
111 Nishiyokotecho, Takasaki

(72) Inventor: Usuke Enomoto
c/o Takasaki Works, Hitachi, Ltd.
111 Nishiyokotecho, Takasaki

(72) Inventor: Atsushi Fujisawa
c/o Hitachi Hokkai Semiconductor, Ltd.
145 Azanakajima, Nanaecho, Kamedagun, Hokkaido

(71) Applicant: Hitachi, Ltd.
4-6 Kandasurugadai, Chiyoda-ku, Tokyo

(71) Applicant: Hitachi Hokkai Semiconductor, Ltd.
1445 [sic] Azanakajima, Nanaecho, Kamedagun, Hokkaido

(74) Agent: Patent Attorney Katsuo Ogawa and one other

Specification

1. Title of the Invention

Electronic device

2. Claims

1. An electronic device comprising:

(1) a semiconductor chip;

(2) a first external connecting terminal connected to a predetermined terminal of said semiconductor chip;

(3) a second external connecting terminal of a planar shape and of a larger surface area than said first external connecting terminal, having an opening formed in a portion thereof, providing heat dissipation and serving as a connecting terminal for said semiconductor chip that is electroconductively attached to a portion of said planar portion; and

(4) a packaging material that becomes an integral unit [by joining] through said opening for the purpose of joining, at the outer peripheral areas of said first and second external connecting terminals and at a gap that is formed between said first and second external connecting terminals;

wherein said first and second external connecting terminals are formed to be surface mountable and said second external connecting terminal is joined outside of the packaging material.

3. Detailed Description of the Invention

(Field of Industrial Use)

[1] The present invention relates to a technology that is effective when used with electronic devices and especially with semiconductor integrated circuits, transistors and the like that generate much heat and are surface mounted.

(Prior Art)

[2] Electronic devices such as the aforementioned semiconductor integrated circuits include dual inline electronic devices, which are formed with a plurality of external connecting terminals that protrude from a package and are inserted into and soldered to insertion holes that are formed

on printed boards.

[3] However, for reasons such as mounting ease, higher mounting density and downsizing of electronic devices, surface mounted electronic devices are now starting to appear in the marketplace as described in "Solid State Technology Japan Edition" (September 1982, pp. 69-77).

[4] [Surface mounted electronic devices] can be summarized as having external connecting terminals that protrude from the side surfaces of a package, which are first bent downward and then bent horizontally at their tips.

[5] The present inventors conducted various studies to improve the heat dissipation of surface mounted electronic devices and furthermore to improve the mechanical strength when mounted. Described below is a technology that is not publicly known but is a technology that was studied by the present inventors. Its overview is as follows.

[6] To explain, the external connecting terminals themselves of surface mounted electronic devices are shaped to be small, and the distance between terminals is also small. Furthermore, [surface mounted electronic devices] can be easily automatically mounted using mounting equipment.

[7] At the same time, electronic devices of large power consumption such as power transistors have been developed. However, with electronic devices of these types, the semiconductor chip generates much heat, and the semiconductor chip needs to be mounted in packages having good heat dissipation.

(Problems to Be Solved by the Invention)

[8] Studies by the present inventors have revealed that external connecting terminals of surface mounted electronic devices are made fine and small to achieve a high mounting density, that the external connecting terminals deform easily for that reason, and that the very small distance between the terminals raises a very high possibility of the occurrence of unexpected accidents such as short-circuits.

[9] Furthermore, it has been revealed that, because of the small surface area of the external connecting terminals of surface mounted electronic devices, the external connecting terminals serve almost no heat dissipation function and that surface mounting type packages cannot be easily used with electronic devices such as power transistors that generate a large amount of heat.

[10] It is the object of the present invention to provide an electronic device having improved mechanical strength and an improved heat dissipation effect when mounted.

[11] The afore-described object and other objects of the present invention shall become clear from the description of the present specification and the attached figures.

(Means for Solving the Problems)

[12] An overview of the representative examples of the invention that is disclosed in the present application is briefly described below. To explain, an external connecting terminal having a heat dissipation effect and to which a semiconductor chip that generates much heat is electroconductively attached is made to have a surface area that is larger than the surface area of other external connecting terminals and is furthermore bent to be surface mountable. Furthermore, formed in the aforesaid external connecting terminal having a heat dissipation effect is an opening through which resin that serves as a packaging material can join.

(Operation)

[13] According to the means described above, heat that is generated by a semiconductor chip is dissipated into atmosphere via the external connecting terminal having a large surface area. Furthermore, because of the large surface area, the soldering area becomes large, which improves mechanical strength when mounted, and the amount of packaging material that fuses into an integral unit through the aforesaid opening becomes large, thus achieving the objects of the present invention of improving the mechanical strength and heat dissipation effect when the electronic device is mounted.

(Embodiment 1)

[14] A first embodiment of an electronic device using the present invention is described next with reference to FIG. 1 through FIG. 3. FIG. 1 is a plan view showing the structure of an electronic device before cutting the external connecting terminals and before encapsulation by a resin mold. FIG. 2 shows one side view, and FIG. 3 shows a perspective view.

[15] As FIG. 1 shows, the source electrode and gate electrode on semiconductor chip 1 are each connected to first external connecting terminals 2, 3 via separate metal thin wires 10, 10.

[16] What should be noted here is the shape of what is referred to in the present invention as

the second external connecting terminal 4. The external connecting terminal 4 is joined together outside of the resin encapsulant 6, is planar shaped with a large surface area as compared to the aforesaid first external connecting terminals 2, 3, and has an opening 5 formed in a portion thereof. A semiconductor chip 1 is attached to a portion of external connecting terminal 4 in an electroconductive manner. Since the bottom surface of semiconductor chip 1 serves as a drain, the external connecting terminal 4 serves both as the drain electrode for the electronic device and as a heat dissipation plate.

[17] The long-dashed short-dashed line identifies the outline of package 6 after molding with an epoxy type resin, and a portion [of the package] overlaps with the aforesaid opening 5.

[18] According to the afore-described shape of external connecting terminal 4, its lateral width W_1 is roughly identical to lateral width W_2 when the external connecting terminals 2, 3 are fixed, and the surface area is large. Thus, heat that is generated by semiconductor chip 1 that is operating is efficiently dissipated into atmosphere via external connecting terminal 4.

[19] Furthermore, in terms of mechanical strength, because the external connecting terminal 4 is shaped to be large, it does not easily deform. Furthermore, when the external connecting terminals 2, 3, 4 are cut at regions X and Y indicated by the dotted lines in FIG. 1, and resin encapsulation is done to package as shown by 6 in FIG. 3, upper package portion 6a and lower package portion 6b of package 6 form an integral unit along the outer peripheral portions A, B, gap C and through opening 5. Thus, since the external connecting terminals 2, 3, 4 are strongly sandwiched by the molding resin, moisture resistance of the electronic device itself is improved.

[20] As shown in FIG. 2 and FIG. 3, external connecting terminals 2 through 4 protrude outwardly from package 6 from near the boundary between upper package portion 6a and lower package portion 6b and are then bent downward. The purpose of this is for soldering the tips to a circuit pattern on a printed board (neither of which is illustrated).

[21] Thus, the soldering area of the external connecting terminal 4 becomes large as compared to that of the other external connecting terminals 2, 3, and a strong connection is formed. As a result, the mechanical strength of the mounting is improved, and incidents such as soldering failure and the like are reduced.

[22] Note that if the afore-described surface mounting type electronic device is formed by cutting the external connecting terminals of a dual inline type IC at portions X, Y identified by the dotted lines in FIG. 1, the package structure can be easily changed from a dual inline type to

a surface mounting type, and mounting automation can be achieved.

[23] The effects obtained from the afore-described embodiment are indicated next.

[24] (1) The external connecting terminal of the electronic device is shaped to have a large surface area, and by electroconductively attaching a semiconductor chip to a portion thereof, the heat that is generated by the semiconductor chip is discharged via the aforesaid external connecting terminal with a large surface area, thus providing the effect of improved heat dissipation of the electronic device.

[25] (2) By shaping the external connecting terminal of the electronic device to have a large surface area and by surface mounting one end thereof, an effect that is obtained is increased mechanical strength when mounted due to increased soldering area with a circuit pattern.

[26] (3) Due to afore-described (2), an effect that is obtained is improved reliability due to a reduction in unexpected accidents such as soldering failures and the like.

[27] (4) By using a configuration wherein an opening is formed at a portion of the afore-described external connecting terminal and by using the opening so that the packaging material integrates the electronic device into one, the bonding between the upper and lower package portions is improved, thus providing the effect of improved mechanical strength of the electronic device itself.

(Embodiment 2)

[28] A second embodiment of the present invention is described next with reference to FIG. 4 and FIG. 5.

[29] The difference between this embodiment and the afore-described first embodiment is that the tip of each of the external connecting terminals is bent to make surface mounting easy.

[30] First, to describe the structure shown in FIG. 4, tips 2a, 3a, 4a of external connecting terminals 2, 3, 4 are all bent outwardly. Thus, the lower surface of tips 2a through 4a, that is, the contact surface with the circuit pattern is enlarged, and soldering between the two becomes commensurately stronger.

[31] FIG. 5 shows tips 2a through 4a of the external connecting terminals bent inwardly. In this case, the area of the lower surface of tips 2 a through 4a is increased, and the soldering area with the circuit pattern is enlarged.

[32] Thus, with the structure of the electronic device shown in this embodiment, in addition to

the afore-described effects that are stated in conjunction with the first embodiment:

[33] (5) By bending the tips of the external connecting terminals and increasing the contact area with the circuit pattern, an effect that is provided is reduced soldering failures when mounted.

[34] (6) Because of (5) above, an effect that is obtained is a further increase in the mechanical strength when mounted.

(Embodiment 3)

[35] A third embodiment of the present invention is described next with reference to FIG. 6.

[36] Note that the present embodiment is an application of the structure of the external connecting terminals described in each of the above embodiments to a small outline (hereinafter "SOP") type IC. An SOP type IC comprises a rectangular solid package that is formed of an epoxy type resin with a plurality of external connecting terminals protruding from the longitudinal-direction side surfaces of the package. FIG. 6 shows the use of the present invention with an SOP type IC. With this SOP type IC package 11, external connecting terminals 13, 14 protrude from both longitudinal-direction side surfaces of package 12. The external connecting terminal 14 has a heat dissipation effect, corresponds to external connecting terminal 4 discussed in the afore-described embodiments and is joined to a tab to which a semiconductor chip is fixed inside package 6.

[37] The external connecting terminal 14 is, for example, two external connecting terminals 13 that are integrated into one. With this structure, because of the presence of a portion that joins the two [external connecting terminals 13], the surface area of external connecting terminal 14 becomes more than twice as large as the surface area of the other external connecting terminals 13.

[38] Also, because the tips of external connecting terminals 13, 14 are bent outwardly, the contact area with the circuit pattern is enlarged.

[39] Thus, with the electronic device of the present embodiment, in addition to the effects that are stated in conjunction with each of the afore-described embodiments:

[40] (7) Of the external connecting terminals of an SOP type IC, by integrating a plurality of external connecting terminals into one and by dissipating the heat from the semiconductor chip, an effect that is obtained is improved heat dissipation in an SOP type IC.

[41] Although the invention made by the present inventors are specifically described in terms

of their embodiments, the present invention is not limited to the afore-described embodiments, and needless to say, various modifications are possible without deviating from the gist of the present invention. For example, external connecting terminal 14 that is shown in the third embodiment may be shaped to be further larger as necessary.

[42] In the foregoing description, although the inventions made by the present inventors are described in terms of the background where the inventions would be used, namely, in the use with electronic devices such as MOS transistors, dual inline type ICs and the like, [the invention] is not limited to them and can be widely used with other surface mounting type ICs.

[43] At the least, the present invention can be used with electronic devices where the external connecting terminals are joined

(Effects of the Invention)

[44] The effects provided by the representative examples of the inventions disclosed in the present application can be briefly described as follows.

[45] To explain, of the external connecting terminals of an electronic device, at least the external connecting terminals that are electroconductively connected to a semiconductor chip are joined outside the encapsulant so as to enlarge the shape and increase the mechanical strength while increasing the surface area and increasing the heat dissipation effect. By so configuring, the effects that are obtained are improved heat dissipation and mechanical strength when electronic devices such as ICs and transistors are mounted.

4. Brief Description of the Figures

[46] FIG. 1 through FIG. 3 show a first embodiment of an electronic device where the present invention is used.

[47] FIG. 1 is a plan view showing the structure of an electronic device.

[48] FIG. 2 is one side view showing the external shape of the aforesaid electronic device.

[49] FIG. 3 is a perspective view showing the external shape of the aforesaid electronic device.

[50] FIG. 4 and FIG. 5 show a second embodiment of the present invention.

[51] FIG. 4 is a perspective view showing one example of bending the external connecting terminals.

[52] FIG. 5 is a perspective view showing another example of bending the external connecting terminals.

[53] FIG. 6 is a perspective view of an SOP type IC that is a third embodiment of the present invention.

[54] 1. Semiconductor chip

2, 3, 4, 13, 14. External connecting terminal

5. Opening

6. Package

11. Dual inline type package

Agent: Patent attorney Katsuo Ogawa

FIG. 1

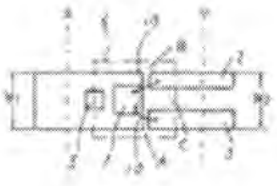


FIG. 4

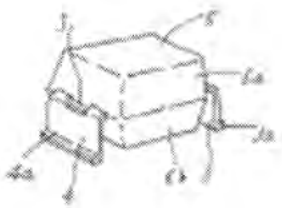


FIG. 2

FIG. 3

[55] 1. Semiconductor chip
2, 3, 4. External connecting terminals
5. Package
X, Y. Cut portion of external connecting terminal

FIG. 5

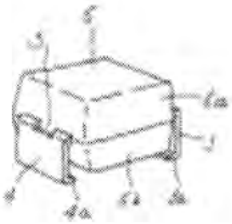
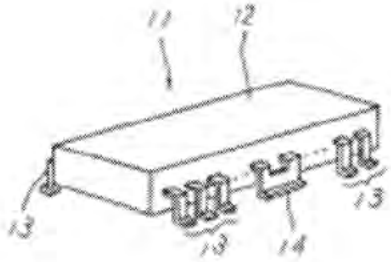


FIG. 6



[56] 11. Dual inline type IC
12. Package
13. External connecting terminal

⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　昭62-206868

⑤Int.Cl.⁴	識別記号	庁内整理番号	⑬公開
H 01 L 23/48		7735-5F	昭和62年(1987)9月11日
23/34		A-6835-5F	

審査請求　未請求　発明の数 1　(全5頁)

⑭発明の名称　電子装置

⑳特　願　昭61-48398
㉒出　願　昭61(1986)3月7日

㉑発明者　大高　成雄　高崎市西横手町111番地　株式会社日立製作所高崎工場内
㉑発明者　復本　宇佑　高崎市西横手町111番地　株式会社日立製作所高崎工場内
㉑発明者　藤沢　敦　北海道亀田郡七飯町字中島145番地　日立北海セミコンダクタ株式会社内
㉑出願人　株式会社日立製作所　東京都千代田区神田駿河台4丁目6番地
㉑出願人　日立北海セミコンダクタ株式会社　北海道亀田郡七飯町字中島1445番地
㉔代理人　弁理士　小川　勝男　外1名

明　細　書

1. 発明の名称

電子装置

2. 特許請求の範囲

1. (1) 半導体チップと、

(2) 上記半導体チップの所定の端子に接続される第1の外部接続端子と、

(3) 上記第1の外部接続端子に対し表面積大の板状になされるとともに、一部に開口部が形成され、かつ板状部の一部に導電可能に接着される上記半導体チップの放熱と外部接続用端子とを兼ねる第2の外部接続端子と、

(4) 上記連結用開口部と上記第1および第2の外部接続端子の外周部、ならびに上記第1および第2の外部接続端子の間に形成される空隙において一体になされるパッケージ材と、

を具備し、前記第1，第2の外部接続端子は面付け実装可能に加工が施されているとともに、前記第2の外部接続端子はパッケージ材外部で連結していることを特徴とする電子装置。

3. 発明の詳細な説明

〔産業上の利用分野〕

本発明は電子装置、特に面付け実装される半導体集積回路、発熱量の大きなトランジスタ等に利用して有効な技術に関する。

〔従来の技術〕

上記半導体集積回路の如き電子装置には、パッケージから突出した複数の外部接続端子をプリント基板に形成された挿通孔に挿入し、半田付けするように形成したデュアルインライン型電子装置がある。

しかし実装の容易化，実装密度の向上、更に電子装置の小型化等があいまって、「Solid State Technology日本版」(September 1982、pp69～77)に記載されているように面付け実装型の電子装置が次第に市場に出回るようになってきた。

その概要は、パッケージの側面から突出した外部接続端子を、下方に折り曲げ、その先端を更に

水平方向に折り曲げたものである。

本発明者等は、上記面付け実装型電子装置の放熱、更に実装時の機械的強度の向上を図るべく種々の検討を行った。以下は、公知とされた技術ではないが、本発明者等によって検討された技術であり、その概要は次のとおりである。

すなわち、面付け実装型の電子装置は、外部接続端子自体の形状が小さく、端子間の距離も小である。さらに、実装装置による自動実装も容易である。

一方、パワートランジスタの如き消費電力が大きい電子装置も開発されているが、この種の電子装置では半導体チップの発熱量も大きく、放熱性の良いパッケージに半導体チップを搭載する必要がある。

〔発明が解決しようとする問題点〕

本発明者等の検討によると、面付け実装型の電子装置は高密度実装化を達成するため外部接続端子が細く小さい。そのため、外部接続端子は変形し易く、しかも端子間距離が微小であるから短絡等の不測の事故が発生する可能性が大きいことが明らかになった。

更に、面付け実装型の電子装置は外部接続端子の表面積が小であるから、放熱機能を殆ど果し得ず、パワートランジスタの如き発熱量の大きな電子装置は面付け実装型のパッケージに成しずらいことも明らかになった。

本発明の目的は、実装時における機械的強度の向上と放熱効果の向上とを図り得る電子装置を提供することにある。

本発明の上記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

〔問題点を解決するための手段〕

本願において開示される発明のうちの代表的なものの概要を簡単に述べれば、下記の通りである。

すなわち、発熱量の大きな半導体チップが導電可能に接着されて放熱効果を有する外部接続端子の表面積を他の外部接続端子の表面積より大きくし、更に面付け実装可能に折り曲げるとともに樹脂からなるパッケージ材が連結する開口部を上記放熱効果を有する外部接続端子に形成するものである。

〔作　用〕

上記した手段によれば、半導体チップから発生した熱は、表面積大の外部接続端子を介して空中に放熱される。更に表面積大であるから半田付け面積が大になり、実装時の機械的強度が向上するとともに、上記開口部を介してパッケージ材の一体となる量が大になる。依って、電子装置の実装時の機械的強度と、放熱効果を向上せしめるという本発明の目的を達成することができる。

〔実施例－１〕

以下、第１図～第３図を介して本発明を適用した電子装置の第１実施例を説明する。なお、第１図は樹脂モールド前の外部接続端子切断前の電子装置の構造を示す平面図、第２図は一側面図、第３図は斜視図を示すものである。

第１図に示すように、半導体チップ１上のソース、電極及びゲート電極は各々が個別の金属細線１０，１０を介して第１の外部接続端子２，３に接続されている。

ここで注目すべきは、本発明でいう第２の外部接続端子４の形状である。外部接続端子４は、樹脂封止体６外部において連結されており、上記第１の外部接続端子２，３に対し表面積大の板状であり、その一部に開口部５が形成されている。外部接続端子４の一部には、半導体チップ１が導電可能に接着されている。半導体チップ１の底面はドレインとなっているので、外部接続端子４は電子装置のドレイン電極となるとともに放熱板ともなる。

一点鎖線は、エポキシ系樹脂による樹脂モールド後のパッケージ６の外形をしめすものであり、一部は上記開口部５にかかっている。

外部接続端子４の上記形状によると、その横幅W_1が外部接続端子２，３が固定されたときの横幅W_2とほぼ同一とし、表面積を大きくする。したがって、動作中の半導体チップ１から発生した熱は、外部接続端子４を介して効率よく空気中に

放熱される。

更に機械的強度についてみると、外部接続端子4は形状大であるから容易に変形しない。そして樹脂封止後の外部接続端子2，3，4を第1図に点線で示すX，Y部分で切断した状態を第2図および第3図に示すようにパッケージ6がなされた場合、パッケージ6のパッケージ上方6aとパッケージ下部6bとは、第1図に示す外部接続端子2，3，4の外周部A，B更に間隙C、更に開口部5において一体になされる。したがって、外部接続端子2，3，4はモールド樹脂によって強固に挟まれているため電子装置自体の耐湿性が向上されることになる。

ところで、外部接続端子2～4は、第2図および第3図に示すように、パッケージ上部6aとパッケージ下部6bとの境界付近からパッケージ6外に突出し、ついで下方に折り曲げられている。これは先端部においてプリント基板の回路パターン（何れも図示せず）に半田付けするためである。

したがって、外部接続端子4の半田付け面積は、他の外部接続端子2，3に比較して大きく、両者の接続が強固になる。この結果、実装時の機械的強度が向上するとともに、半田付け不良等の事故を低減することもできる。

尚、上記した面付け実装型電子装置はデュアルインライン型ICの外部接続端子を第1図の点線で示すX，Y部分で切断し形成すると、デュアルインライン型から面付実装型にパッケージ構造を容易に変更でき、実装の自動化が達成できる。

上記した実施例によって得られる効果を下記に示す。

(1) 電子装置の外部接続端子を表面積大の形状になし、その一部に半導体チップを導電可能に接着することにより、上記半導体チップから発生した熱を上記表面積大の外部接続端子を介して放出するという作用で、電子装置の放熱効果が向上するという効果が得られる。

(2) 電子装置の外部接続端子を表面積大の形状になし、その一端を面付け実装することにより、回路パターンとの半田付け面積が拡大するという作用で、実装時の機械的強度が向上する、という効果が得られる。

(3) 上記(2)により、半田付け不良等の不測の事故が低減されるので、信頼性が向上する、という効果が得られる。

(4) 上記外部接続端子の一部に開口部を形成し、電子装置のパッケージ材の一部がこの開口部を介して一体になされるように構成したことにより、上下パッケージの結合度が大になるという作用で、電子装置自体の機械的強度が向上する、という効果が得られる。

〔実施例－2〕

次に、第4図および第5図を参照して本発明の第2実施例を説明する。

なお、本実施例と上記第1実施例との相違点は、各外部接続端子の先端部を折り曲げて、面付け実装を容易にしたことにある。

先ず、第4図に示す構造から述べると、外部接続端子2，3，4の先端部2a，3a，4aが、図示のように互いに外側方向に折り曲げられている。したがって、先端部2a～4aの下側面、換言すれば回路パターンとの接触面積が拡大され、この分両者の半田付けが強固になる。

第5図は外部接続端子の先端部2a～4aを互いに内側方向に折り曲げたものである。この場合も先端部2a～4aの下側面の面積が大になり、回路パターンとの半田付け面積が拡大される。

したがって、本実施例に示した電子装置の構造によれば、上記第1実施例で述べた効果を奏するうえに、

(5) 外部接続端子の先端部を折り曲げ、回路パターンとの接触面積を大にすることにより、実装時の半田付け不良が低減される、という効果が得られる。

(6) 上記(5)により、実装時の機械的強度がより一層増大する、という効果が得られる。

〔実施例－3〕

次に、第6図を参照して本発明の第3実施例を説明する。

なお、本実施例は上記各実施例で述べた外部接

続端子の構造をスモールアウトライン（以下ＳＯＰ）型ＩＣに適用したものである。尚、ＳＯＰ型ＩＣはエポキシ系樹脂により形成された長方体のパッケージとこのパッケージの長手方向両側面から突出する複数の外部接続端子からなっている。第６図は本発明をこのＳＯＰ型ＩＣに適用したものであり、このＳＯＰ型ＩＣパッケージ１１は、パッケージ１２の長手方向の両側面から外部接続端子１３，１４が突出している。外部接続端子14は放熱効果を有しており、上記実施例で述べた外部接続端子４に相当するものであり、パッケージ６内において半導体チップが固定されるタブと連結している。

外部接続端子１４は、外部接続端子１３のたとえば２本分を一体にしたものである。この構造によると、両者の結合部分があるので、外部接続端子１４の表面積は他の外部接続端子１３の表面積と比較して２倍以上になる。

また、外部接続端子１３，１４の先端部はそれぞれ外側方向に折り曲げられているので、回路パターンとの接触面積が拡大される。

したがって本実施例に示す電子装置は、上記各実施例で述べた効果を奏するうえに、

(7) ＳＯＰ型ＩＣの外部接続端子のうち複数の外部接続端子を一体になし、半導体チップの放熱をおこなわしめることにより、ＳＯＰ型ＩＣの放熱効果を向上させる、という効果が得られる。

以上に、本発明者によってなされた発明を実施例にもとづき具体的に説明したが、本発明は上記実施例に限定されるものではなく、その要旨を逸脱しない範囲で種々変形可能であることはいうまでもない。たとえば、第３実施例で示した外部接続端子１４は必要に応じて形状を更に大にしてもよい。

以上の説明では、主として本発明者等によってなされた発明をその背景となった利用分野であるＭＯＳトランジスタ、デュアルインライン型ＩＣ等の電子装置に適用した場合について説明したが、それに限定されるものではなく、他の面付け実施型ＩＣに広く利用することができる。

本発明は少なくとも、外部接続端子が連結している電子装置に利用できる。

〔発明の効果〕

本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば、下記のとおりである。

すなわち、電子装置の外部接続端子のうち少なくとも半導体チップに導通可能に接続された外部接続端子を封止体外部で連結して、形状大として機械的強度を増大せしめるとともに、表面積を大にして放熱効果を向上せしめるように構成したので、ＩＣ，トランジスタの如き電子装置の実装時の機械的強度と放熱効果とが向上する、という効果が得られる。

4. 図面の簡単な説明

第１図～第３図は本発明を適用した電子装置の第１実施例を示すものであり、

第１図は電子装置の構造を示す平面図、

第２図は上記電子装置の外形を示す一側面図、

第３図は上記電子装置の外形を示す斜視図、

第４図および第５図は本発明の第２実施例を示すものであり、

第４図は外部接続端子の折り曲げの一例を示す斜視図、

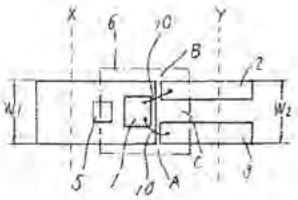
第５図は外部接続端子の折り曲げの他の例を示す斜視図、

第６図は本発明の第３実施例を示すＳＯＰ型ICの斜視図である。

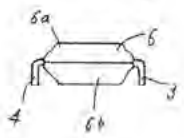
１…半導体チップ、２，３，４，１３，１４…外部接続端子、５…開口部、６…パッケージ、11…デュアルインライン型パッケージ。

代理人　弁理士　小川勝男

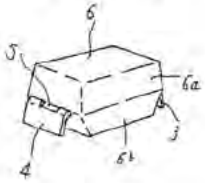
第 1 図



第 2 図

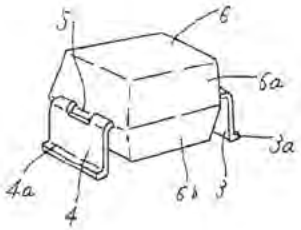


第 3 図

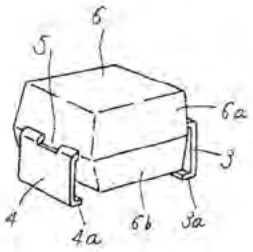


1 — 半導体チップ
2, 3, 4 — 外部接続端子
5 — パッケージ
X, Y — 外部接続端子切断部

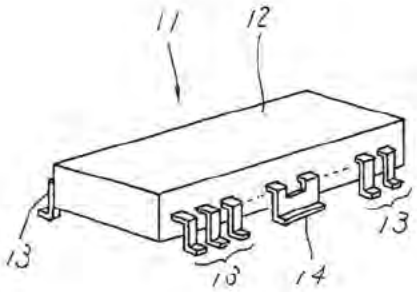
第 4 図



第 5 図



第 6 図



11 — デュアルインライン型IC
12 — パッケージ
13 — 外部接続端子

EXHIBIT 10

(19) Japan Patent Office (JP)

(12) **Japanese Unexamined Patent Application Publication** (A)

(11) Japanese Unexamined Patent Application Publication Number

H4-225268

(43) Publication date: August 14, 1992

(51) Int. Cl.[5]	Identification codes	JPO file numbers	FI	Technical indications
H01L 23/50	F	8418-4M		
23/34	A	7220-4M		

Request for examination: Not yet requested Number of claims: 1 (Total of 5 pages)

(21) Application number: Japanese Patent Application H2-414445

(22) Date of application: December 26, 1990

(71) Applicant: 000003078
Toshiba Corporation
72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken

(71) Applicant: 000221199
Toshiba Microelectronics Corporation
25-1 Ekimaehon-cho, Kawasaki-ku, Kawasaki-shi, Kanagawa-ken

(72) Inventor: Toru IIYAMA
c/o Toshiba Tamagawa Works
1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken

(72) Inventor: Satoru ITAKURA
c/o Toshiba Microelectronics Corporation
25-1 Ekimaehon-cho, Kawasaki-ku, Kawasaki-shi, Kanagawa-ken

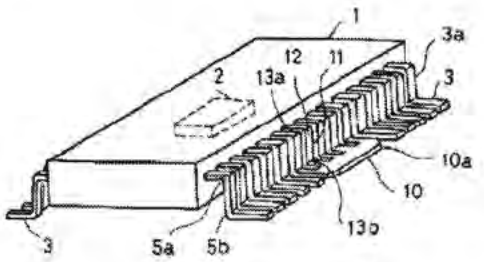
(74) Agent: Patent Attorney Norio OHGO

(54) (TITLE OF THE INVENTION) Semiconductor device

(57) (ABSTRACT)

(PROBLEM) Prevent cracking of the enclosure and detachment at the interface between the enclosure and the heat sink, providing quality that remains stable even over time, without circuit damage, in a semiconductor device capable of being mounted by bending the heat sink together with the leads, etc.

(MEANS FOR SOLVING) In a semiconductor device furnished with leads 3 electrically connected to a semiconductor chip 3 housed within a resin-molded enclosure and a heat sink 10 formed wider than leads 3 that is thermally connected to semiconductor chip 2, wherein bends 5a, 13a are provided at a portion 3a, 10a of leads 3 and heat sink 10 projecting from enclosure 1, aperture part 11 is formed in heat sink 10 at bend 13a in such a way as to form a crossover part 12 that is essentially the same width as the leads 3.



(SCOPE OF PATENT CLAIMS)
(CLAIM 1) Semiconductor device furnished with an enclosure resin-molded to house a semiconductor chip, leads electrically connected to the aforesaid semiconductor chip within this enclosure, and heat sink formed wider than these leads that is thermally connected to the aforesaid semiconductor chip, wherein bends are provided at a portion of each of the aforesaid leads and heat sink projecting from the aforesaid enclosure, characterized in that an aperture part is formed in the aforesaid heat sink at the aforesaid bend in such a way as to form a crossover part that is essentially the same width as the aforesaid leads.
(DETAILED DESCRIPTION OF THE INVENTION)
[OBJECTIVE OF THE INVENTION]
(0001)
(FIELD OF INDUSTRIAL APPLICATION) This invention relates to a semiconductor device wherein a heat sink is provided in such a way as to project to the exterior of an enclosure formed by resin molding.
(0002)
(PRIOR ART) As has been known prior to now, semiconductor devices with an enclosure made of silicone resin, epoxy resin or the like are widely used in semiconductor device consumer applications and the like due to their ease of manufacture. Additionally, in semiconductor devices with low power consumption of on the order of several W, the same metal plate frame used for the leads that provide the electrical connection is used to form a wide heat sink.
(0003) One example of a prior-art semiconductor device will be described below referencing FIG. 5 and FIG. 6. FIG. 5 is a perspective view and FIG. 6 is a plane view of the lead frame.
(0004) In the drawings, 1 is an enclosure formed into a roughly rectangular solid shape by resin molding, the interior of which enclosure 1 hermetically houses a semiconductor chip 2 on which an integrated circuit, for example, has been formed. On the interior of enclosure 1, the terminals of semiconductor chip 2 and are electrically connected to the leads 3 by bonding wire, and semiconductor chip 2 is thermally connected to heat sink 4, which is wider than lead 3.
(0005) Furthermore, a plurality of leads 3 and a heat sink 4 are provided in such a way as to pass through the long side wall of enclosure 1 from the interior to the exterior. Additionally, leads 3 and heat sink 4 each have bends 5a, 5b, 6a, 6b at two locations on their respective portions 3a, 4a extending from enclosure 1, and are formed in such a way as to enable surface mounting onto a circuit board or the like, for example.
(0006) The production of a semiconductor device configured in this manner can be carried out by forming leads 3 and heat sink 4 into a lead frame 7 from the same metal plate, connecting a semiconductor chip 2 to this lead frame 7, hermetically housing semiconductor chip 2 by resin-molding an enclosure 1, and then bending these leads 3 and heat sink 4 into a designated shape and, in the same process, trimming off the dam bar 8 connecting each of these while forming leads 3 and heat sink 4 into the designated dimensions and shape.
(0007) However, in the aforesaid prior art, when bending portions 3a, 4a of leads 3 and heat sink 4 projecting to the exterior of enclosure 1 into the designated shape, heat sink 4 is formed to a broad width several times that of lead 3, rendering it easy to apply excessive force to the portion where heat sink 4 projects from enclosure 1, which runs the risk of causing detachment at the interface between the resin of enclosure 1 and the metal of heat sink 4 at this projecting portion of heat sink 4, or cracking in the vicinity of the location where heat sink 4 projects from enclosure 1. Furthermore, stability was lacking in regards to the bending dimensions.
(0008) What's more, the above-stated risk of detachment or cracking near the interface was particularly great when simultaneously bending both projecting portions 3a, 4a of leads 3 and heat sink 4, which typically have different widths, or when positioning bends 5a, 6a closer to enclosure 1 in order to reduce space occupancy for mounting on a circuit board.
(0009) If detachment or cracking occurs at the interface, air, water or the like can enter into the enclosure 1 through the gap at the site of the detachment or cracking, adhering to and fouling the semiconductor chip 2 hermetically housed therein, damaging the circuit formed on the chip, impairing performance, etc. Even microscopic detachment or cracking could cause problems such as fouling of the semiconductor chip 2 or the like at a later date due to the gradual widening of the detachment or cracking.
(0010) Furthermore, bending the leads 3 and heat sink 4 in separate processes so as to prevent detachment or cracking at the interface, or placing the bend 6a in heat sink 4 further away from enclosure 1, would reduce manufacturing efficiency or increase mounting area requirements.
(0011)
(PROBLEM TO BE SOLVED BY THE INVENTION) This invention was devised to address the problem described above, whereby detachment or cracking can occur at the interface in prior-art devices as a result of bending the heat sink, potentially causing a variety of problems, having as its objective to provide a semiconductor device wherein cracking of the enclosure and detachment at the interface between the enclosure and the heat sink does not occur, thereby ensuring that quality remains stable even over time, without circuit damage, and doing so without reducing manufacturing efficiency or mounting efficiency.
(0012) [Configuration of the invention]
(0013)
(MEANS OF SOLVING THE PROBLEM) The semiconductor device of this invention is characterized in that, in a semiconductor device furnished with an enclosure resin-molded to house a semiconductor chip, leads electrically connected to the aforesaid semiconductor chip within this enclosure, and heat sink formed wider than these leads that is thermally connected to the aforesaid semiconductor chip, wherein bends are provided at a portion of each of the aforesaid leads and heat sink projecting from the aforesaid enclosure, an aperture part is formed in the aforesaid heat sink at the aforesaid bend in such a way as to form a crossover part that is essentially the same width as the aforesaid leads.
(0014)
(ACTION) In a semiconductor device configured in the manner described above, an aperture part is formed at the

bend in the heat sink in such a way as to form a crossover part that is essentially the same width as the leads, and for this reason, the bend width of the bend in the heat sink is a repeat of essentially the same bend width as the leads, thereby making it possible to perform bending at a uniform bending force. This in turn makes it possible to place the bend location near the workable side wall of the enclosure in both the leads and the heat sink so as to eliminate local force from acting on the enclosure, thus preventing detachment from occurring at the interface between the heat sink and the resin of the enclosure, and providing for stable quality over time without circuit damage.

(0015)

(EMBODIMENT EXAMPLES) Embodiment examples of the present invention will be described below referencing FIG. 1 through FIG. 4. Moreover, components identical to the prior art will be indicated with the same symbol and will not be described, with only components of the present invention that differ from the prior art being described.

(0016) First, the first embodiment example will be described by means of FIG. 1 and FIG. 2. FIG. 1 is a perspective view and FIG. 2 is a plane view of the lead frame.

(0017) In the drawings, 10 is a heat sink provided in such a way as to project from the central portion of the side wall of enclosure 1, as in the prior art, to which a semiconductor chip 2 hermetically housed in enclosure 1 is thermally connected. Four rectangular aperture parts 11 and five crossover parts 12 with essentially the same width as the leads 3 are formed in parallel from the interior to the exterior of enclosure 1 in the projection direction of heat sink 10.

(0018) Additionally, projecting portion 10a of heat sink 10 is bent at the same location as lead 3, being bent into an S shape with two essentially right-angled bends 13a, 13b. Moreover, the two bends 13a, 13b are both formed by bending crossover part 12.

(0019) As in the prior art, the device in this embodiment example formed in this way can be produced using a lead frame 14 formed by stamping or etching the leads 3, heat sink 10, aperture part 11, etc. into the same metal plate. The production process for this embodiment example is the same as the prior art, and involves connecting the inner end of enclosure 1 of lead frame 14 to the terminal of semiconductor chip 2 with bonding wire, followed by hermetically housing semiconductor chip 2 by resin-molding of enclosure 1.

(0020) The areas near the base of projecting portions 3a, 10a of leads 3 and heat sink 10 where these project from enclosure 1 are deemed first bends 5a, 13, and are simultaneously bent into an S shape while, in the same process, the dam bar 8 connecting each is cut as leads 3 and heat sink 10 are molded to the designated dimensions and shape.

(0021) According to the above-described embodiment example, the bend width of the two bends 13a, 13b in heat sink 10 are a repeat of essentially the same bend width as the leads 3, causing all to be bent by the action of a uniform bending force. In regards to the bending location, too, the same location near the workable side wall of enclosure 1 can be used for both leads 3 and heat sink 10, thereby preventing local force from acting on enclosure 1, from which leads 3 and heat sink 10 project, as well as preventing major detachment force from acting on the interface between the heat sink 10 and the resin of enclosure 1.

(0022) For this reason, cracking of enclosure 1 or peeling at the interface does not occur. Furthermore, this also prevents air, water or the like from entering into the interior of enclosure 1 and adhering to and fouling the hermetically housed semiconductor chip 2, which could damage the circuit formed on the chip, impair performance, etc. Additionally, problems do not arise due to fouling of the semiconductor chip 2 or the like caused by the growth of detachment or cracks over time.

(0023) Furthermore, the bending of leads 3 and heat sink 10 can be simultaneously performed at a bend location close to enclosure 1, providing for stable bend dimensions, which prevents reduction of manufacturing efficiency, eliminates the need to increase the mounting area, etc.

(0024) Next, a second embodiment example will be described referencing FIG. 3 and FIG. 4. FIG. 3 is a perspective view and FIG. 4 is a plane view of the lead frame.

(0025) In the drawings, as in the case of the first embodiment example, 15 is a heat sink provided in such a way as to project from the central portion of the side wall of enclosure 1, to which a semiconductor chip 2 hermetically housed in enclosure 1 is thermally connected. The projecting portion 15a of heat sink 15 is bent into an S shape, with two essentially right-angled bends 16a, 16b at the same bend location as the leads 3. Additionally, four aperture parts 18a, 18b are formed at the bend peak of each of bends 16a, 16b in heat sink 15 in such a way as to form five crossover parts 17a, 17b having essentially the same width as the leads 3.

(0026) As in the case of embodiment example 1, the device in this embodiment example formed in this way can be produced using a lead frame 19 on which the leads 3, heat sink 15, aperture parts 18a, 18b, etc. have been formed on the same metal plate. As in the case of the first embodiment example, the production process for this embodiment example involves connecting a semiconductor chip 2 to a lead frame 19, followed by formation of an enclosure 1 by resin molding.

(0027) Additionally, leads 3 and heat sink 15 are simultaneously bent into an S shape at a designated location on projection portions 3a, 15a and, in the same process, leads 3 and heat sink 15 are molded to the designated dimensions and shape, and the dam bar 8 connecting each of these is trimmed off.

(0028) The aforesaid embodiment example has the same action and effect as the first embodiment example, and because it involves the formation of the minimum aperture parts 18a, 18b required by bends 16a, 16b, is able to suppress reduction of the heat radiation effect.

(0029) Moreover, the present invention is not limited to the above-described embodiment examples, and can be modified appropriately as long this is done in a way that does not deviate from the essence of the invention.

(0030)

(EFFECT OF THE INVENTION) As the above description makes clear, because aperture parts are formed in such a way as to form a crossover part having essentially the same width as the leads on the bend of the heat sink, the present invention has the following effect. Namely, the present invention has the effect of preventing cracking of the enclosure and detachment at the interface between the enclosure and the

heat sink, thereby ensuring that quality remains stable even over time, without circuit damage, and doing so without reducing manufacturing efficiency or mounting efficiency.

(BRIEF DESCRIPTION OF THE DRAWINGS)

(FIG. 1) Perspective view showing the first embodiment example of the present invention.

(FIG. 2) Plane view of the lead frame in the first embodiment example.

(FIG. 3) Perspective view showing the second embodiment example of the present invention.

(FIG. 4) Plane view of the lead frame in the second embodiment example.

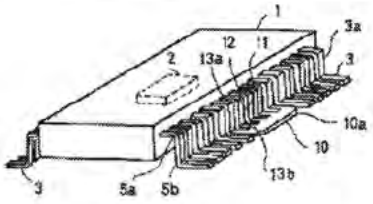
(FIG. 5) Perspective view showing a prior-art example.

(FIG. 6) Plane view of the lead frame in a prior-art example.

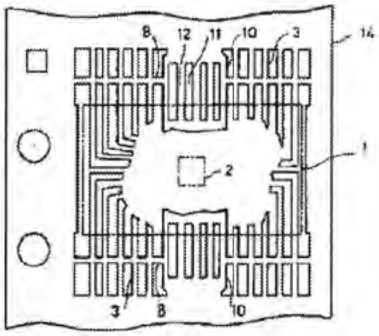
(DESCRIPTION OF THE SYMBOLS)

1: Enclosure
2: Semiconductor chip
3: Leads
3a: Projecting portion of leads
10: Heat sink
10a: Projecting portion of heat sink
11: Aperture part
12: Crossover part
13a, 13b: Bend in heat sink

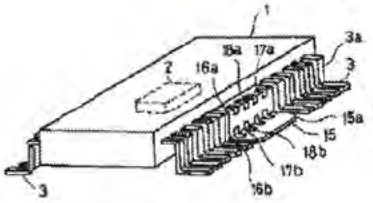
(FIG. 1)



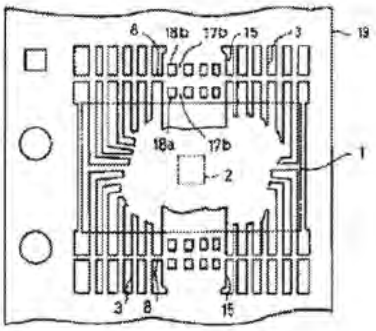
(FIG. 2)



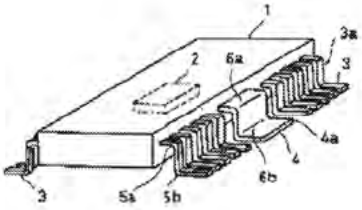
(FIG. 3)



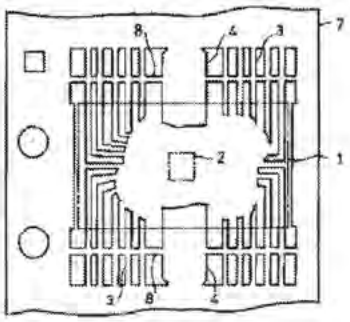
(FIG. 4)



(FIG. 5)



(FIG. 6)



TRANSPERFECT

I attest that the attached document is a true and accurate translation of JPH04225268A.

I performed the proofreading and am fluent in English and Japanese.

I understand that wilful false statements and the like are punishable by fine or imprisonment or both. These statements are true and are made of my own knowledge.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on 27 December 2017 at Bethesda, MD

Signed

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平4－225268

(43)公開日　平成４年(1992)８月14日

(51)Int.Cl.[5]	識別記号	庁内整理番号	Ｆ１	技術表示箇所
Ｈ０１Ｌ　23/50		Ｆ　8418－4Ｍ		
23/34		Ａ　7220－4Ｍ		

審査請求　未請求　請求項の数１（全　５　頁）

(21)出願番号　特願平2－414445

(22)出願日　平成２年(1990)12月26日

(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地

(71)出願人　000221199
東芝マイクロエレクトロニクス株式会社
神奈川県川崎市川崎区駅前本町25番地１

(72)発明者　飯山　徹
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝多摩川工場内

(72)発明者　板倉　悟
神奈川県川崎市川崎区駅前本町25番地１
東芝マイクロエレクトロニクス株式会社内

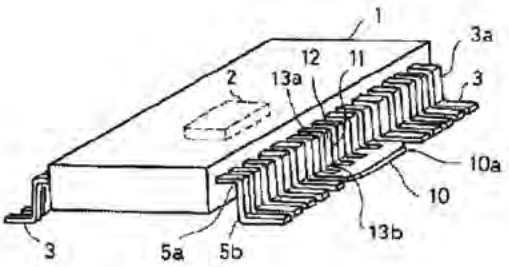
(74)代理人　弁理士　大胡　典夫

(54)【発明の名称】　半導体装置

(57)【要約】

【目的】　リードと共に放熱板を曲げて実装等が出来るようにするものについて、外囲器の割れや、外囲器と放熱板との界面での剥離が発生せず、回路破壊のない、経時的にも安定した品質が得られるものにする。

【構成】　樹脂成形された外囲器１内に収納した半導体チップ２に、電気的に接続したリード３及びリード３より広幅に形成され半導体チップ２に熱的に接続した放熱板10とを備え、リード３及び放熱板10の外囲器１からのそれぞれの延出部分３ａ，10ａに曲部５ａ，13ａが設けられてなるものにおいて、放熱板10は曲部13ａにリード３と略同幅の渡り部12が形成されるように開孔部11が形成されている。



1

【特許請求の範囲】

【請求項1】 半導体チップを収納して樹脂成形された外囲器と、この外囲器内で前記半導体チップに電気的に接続したリード及びこのリードより広幅に形成され前記半導体チップに熱的に接続した放熱板とを備え、前記リード及び放熱板の前記外囲器からのそれぞれの延出部分に曲部が設けられてなるものにおいて、前記放熱板は前記曲部に前記リードと略同幅の渡り部が形成されるように開孔部が形成されていることを特徴とする半導体装置。

【発明の詳細な説明】

［発明の目的］

【0001】

【産業上の利用分野】本発明は、樹脂成形によって形成した外囲器外に延出するように放熱板が設けられた半導体装置に関する。

【0002】

【従来の技術】従来より知られているように、外囲器をシリコーン樹脂やエポキシ樹脂などで形成した半導体装置は製造が容易な点から民生用の半導体装置等として多量に使用されている。そして消費電力が数W程度となるものでは電気接続を行うリードと同じ金属板のフレームを用いて広幅の放熱板を形成している。

【0003】以下従来の半導体装置の一つについて図5及び図6を参照して説明する。図5は斜視図であり、図6はリードフレームの平面図である。

【0004】図において1は樹脂成形により略直方体に形成された外囲器であり、この外囲器1の内部には、例えば集積回路が形成された半導体チップ2が密封収納されている。そして外囲器1の内部において、半導体チップ2の端子とリード3がボンディングワイヤによって電気的に接続されており、さらに半導体チップ2とリード3よりも広い幅の放熱板4が熱的に接続されている。

【0005】また、外囲器1の長手の側壁には、内部から外部に向かって貫通するようにして複数のリード3と放熱板4が設けられている。そしてリード3及び放熱板4は、外囲器1から各々の延出部分3a，4aがそれぞれ2カ所に曲部5a，5b，6a，6bを持っており、例えば配線基板等に表面実装できるように形成されている。

【0006】このように構成される半導体装置の作成は、リード3及び放熱板4を同一の金属板にリードフレーム7として形成し、このリードフレーム7に半導体チップ2を接続した後に外囲器1を樹脂成形して半導体チップ2を密封収納し、さらにリード3及び放熱板4を所定形状に曲げ加工すると共に、同じ工程においてリード3及び放熱板4を所定の寸法、形状に成形しながらそれぞれを接続しているダムバー8を切落として行われる。

【0007】しかしながら上記の従来技術においては、外囲器1外に延出したリード3及び放熱板4の延出部分

2

3a，4aを所定の形状に曲げ加工する際、放熱板4は広幅でリード3の数倍の幅を有するように形成されているために、外囲器1の放熱板4が延出している部分に無理な力が加わり易く、この放熱板4が延出している部分での外囲器1の樹脂と放熱板4の金属との界面に剥離が生じたり、外囲器1の放熱板4が延出している部分の近傍にひび割れが生じる虞がある。また曲げ寸法の安定性に欠けていた。

【0008】さらに、効率的な製造を行うために、通常曲げ幅が異なるリード3と放熱板4の延出部分3a，4aを同時に曲げ加工する場合や、さらに配線基板に実装するときの占有面積をより少なくするために曲部5a，6aをより外囲器1に近い位置にとる場合には、特に上述の界面での剥離やひび割れが生じる虞が大きい。

【0009】そして、界面での剥離やひび割れが生じると、剥離やひび割れが生じた部分の隙間から外囲器1内に外気や水などが入り、密封収納された半導体チップ2に付着して汚損し、チップに形成された回路を破壊したり、性能低下を引起こしたり等する。また一度微少の剥離やひび割れが生じた場合には、経時的に剥離やひび割れが進行して半導体チップ2の汚損等の問題を後で生じることとなる。

【0010】また、界面での剥離やひび割れが生じないようにリード3と放熱板4の曲げ加工を別々の工程で行ったり、放熱板4の曲部6aを外囲器1から離した位置にとったりすると、製造効率が低下したり、実装面積が多く必要となったりする。

【0011】

【発明が解決しようとする課題】上記のような従来の装置で放熱板の曲げ加工によって界面で剥離やひび割れが生じ、これに伴い種々の問題が発生する虞がある状況に鑑みて本発明はなされたもので、その目的とするところは、製造効率や実装効率が低下することなく、外囲器の割れや、外囲器と放熱板との界面での剥離が発生せず、回路破壊のない経時的にも安定した品質が得られる半導体装置を提供することにある。

【0012】［発明の構成］

【0013】

【課題を解決するための手段】本発明の半導体装置は、半導体チップを収納して樹脂成形された外囲器と、この外囲器内で半導体チップに電気的に接続したリード及びこのリードより広幅に形成され半導体チップに熱的に接続した放熱板とを備え、リード及び放熱板の外囲器からのそれぞれの延出部分に曲部が設けられてなるものにおいて、放熱板は曲部にリードと略同幅の渡り部が形成されるように開孔部が形成されていることを特徴とするものである。

【0014】

【作用】上記のように構成された半導体装置は、放熱板が曲部にリードと略同幅の渡り部が形成されるように開

孔部を形成しており、このため放熱板の曲部は曲げ幅がリードの曲げ幅と略同じものの繰返しとなっており、均等な曲げ力で曲げることができ、曲げ位置もリードと放熱板は加工可能な外囲器の側壁に近い同じ位置にとることができて外囲器に局部的な力が作用せず、また放熱板と外囲器の樹脂との界面では剥離が生じず、そして回路破壊のない、経時的にも安定した品質のものとなる。

【0015】

【実施例】以下、本発明の実施例を図1乃至図4を参照して説明する。なお、従来と同一部分には同一符号を付して説明を省略し、従来と異なる本発明の構成について説明する。

【0016】先ず第1の実施例を図1及び図2により説明する。図1は斜視図であり、図2はリードフレームの平面図である。

【0017】図において、10は従来例と同様に外囲器1の側壁中間部から延出するように設けられた放熱板で、これには外囲器1内に密封収納された半導体チップ2が熱的に接続されている。放熱板10には延出方向に沿って外囲器1の内側から外側にかけて4本の長方形の開孔部11と、リード3と略同幅の5本の渡り部12が並行して形成されている。

【0018】また、放熱板10は延出部分10aがリード3と曲げ位置を同じくして、2か所の略直角の曲部13a，13bを持ってS字状に曲げられている。なお2か所の曲部13a，13bは共に渡り部12を曲げることによって形成されている。

【0019】このように形成された本実施例の装置は、従来例と同様に同一の金属板にリード3や放熱板10、開孔部11等が打抜き加工、あるいはエッチング加工によって形成されたリードフレーム14を用いて作成される。本実施例の作成工程も従来と同様で、リードフレーム14の外囲器1の内側端部と半導体チップ2の端子とをボンディングワイヤで接続した後に、外囲器1を樹脂成形して半導体チップ2を密封収納する。

【0020】さらにリード3及び放熱板10を、延出部分3a，10aの曲げ加工可能な外囲器1からの延出根元部の近傍を第1の曲部5a，13aとし、同時にS字状に曲げ加工すると共に、同じ工程においてリード3及び放熱板10を所定の寸法、形状に成形しながらそれぞれを接続しているダムバー8を切落とす。

【0021】上述の本実施例によれば、放熱板10の2か所の曲部13a，13bは曲げ幅がリード3の曲げ幅と略同じものの繰返しとなっているために、すべてに均等な曲げ力が作用して曲げられる。そして曲げ位置も、リード3及び放熱板10は共に加工可能な外囲器1の側壁に近い同じ位置にとることができ、リード3及び放熱板10が延出している外囲器1にも局部的な力が作用せず、また放熱板10と外囲器1の樹脂の界面での大きな剥離力が作用しない。

【0022】このため外囲器1のひび割れや界面での剥離が生じない。そして外囲器1内に外気や水などが入り、密封収納された半導体チップ2に付着して汚損し、チップに形成された回路を破壊したり、性能低下を引起こしたり等することがない。さらに経時的に剥離やひび割れが進行することによる半導体チップ2の汚損等の問題が生じることもない。

【0023】また、リード3と放熱板10の曲げ加工を、同時に外囲器1から近い位置に曲げ位置をとって行うことができ、曲げ寸法も安定したものとなり、製造効率を低下させたり、実装面積を多く必要とするようなこと等がなくなる。

【0024】次に、第2の実施例を図3及び図4により説明する。図3は斜視図であり、図4はリードフレームの平面図である。

【0025】図において、15は第1の実施例と同様に外囲器1の側壁中間部から延出するように設けられた放熱板で、これには外囲器1内に密封収納された半導体チップ2が熱的に接続されている。放熱板15は延出部分15aがリード3と曲げ位置を同じくして、2か所の略直角の曲部16a，16bを持ってS字状に曲げられている。そして放熱板15の曲部16a，16bにはそれぞれ曲げ頂部にリード3と略同幅の5本の渡り部17a，17bが形成されるように各4つの開孔部18a，18bが形成されている。

【0026】このように形成される本実施例の装置も、第1の実施例と同様に同一の金属板にリード3や放熱板15、開孔部18a，18b等が形成されたリードフレーム19を用いて作成される。本実施例の作成工程も第1の実施例と同様、リードフレーム19に半導体チップ2を接続した後、樹脂成形により外囲器1を形成する。

【0027】さらにリード3及び放熱板15を、延出部分3a，15aの所定の位置で同時にS字状に曲げ加工し、同じ工程においてリード3及び放熱板15を所定の寸法、形状に成形し、それぞれを接続しているダムバー8を切落とす。

【0028】上記の本実施例においても第1の実施例と同様の作用、効果を有すると共に、曲部16a，16bに必要とする最少限の開孔部18a，18bを形成するように成るため、放熱効果の低減を少なくすることができる。

【0029】尚、本発明は上記の各実施例に限定されるものではなく、要旨を逸脱しない範囲内で適宜変更して実施し得るものである。

【0030】

【発明の効果】以上の説明から明らかなように、本発明は放熱板が曲部にリードと略同幅の渡り部が形成されるように開孔部を形成する構成としたことにより、次のような効果が得られる。即ち製造効率や実装効率を低下させることなく、外囲器の割れや、外囲器と放熱板との界面での剥離の発生を防止でき、回路破壊がない、経時的にも安定した品質が得られる等の効果を奏する。

5

【図面の簡単な説明】

【図１】本発明の第１の実施例を示す斜視図である。

【図２】第１の実施例に係わるリードフレームの平面図である。

【図３】本発明の第２の実施例を示す斜視図である。

【図４】第２の実施例に係わるリードフレームの平面図である。

【図５】従来例を示す斜視図である。

【図６】従来例に係わるリードフレームの平面図である。

6

【符号の説明】

１…外囲器

２…半導体チップ

３…リード

３ａ…リードの延出部分

10…放熱板

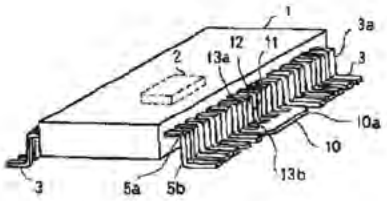
10ａ…放熱板の延出部分

11…開孔部

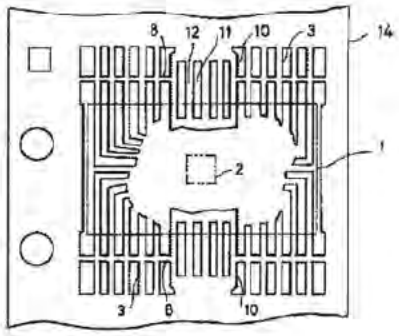
12…渡り部

13ａ，13ｂ…放熱板の曲部

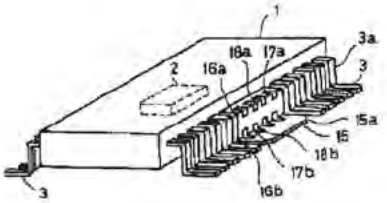
【図１】



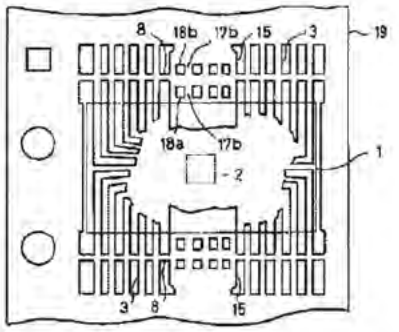
【図２】



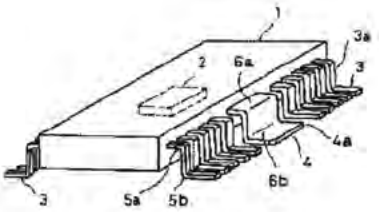
【図３】



【図４】



【図５】



【図6】

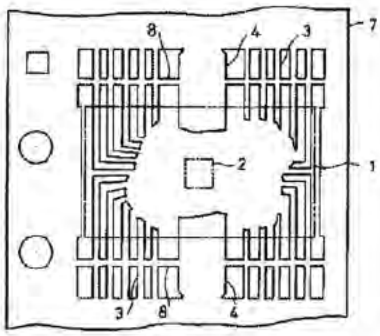


EXHIBIT 11

An Optimization Study of Thermal Path from Plastic Packages to Board

Chin C. Lee, David H. Chien, and Chen S. Tsai
Electrical and Computer Engineering Department
2226 Engineering Gateway Building
University of California
Irvine, California 92697
Phone: 714-824-7462
Fax: 714-824-3732
e-mail: cclee@uci.edu

Abstract

A study is carried out to optimize the thermal path from plastic packages to Printed Circuit Board (PCB). Various thermal enhancement features are investigated in this work to improve the thermal path. This effort results in a new leadframe design of which the die-pad region is indented to expose its bottom surface to the package exterior. The potential advantages of this indented leadframe package are: 1) the exposed die-pad surface can be soldered to a thermal via in the printed circuit board, thus providing the shortest possible thermal path from the die to the board, 2) the additional solder joint greatly enhances the mechanical strength and reliability of the PCB assembly, 3) since the die surface is almost in plane with bonding pads on the leadframe, wire bonding process is easier and the wires can be shortened to reduce inductance, and 4) being soldered to the PCB, the die-pad region also serves as the best possible electrical ground. Since the exposed die-pad is mounted in the same soldering operation as the leads during assembly, the extra cost of the above improvements is due to a few extra stamping steps for the die pad indentation. Thus, this new package design can be implemented at low cost. Finite Element analysis has been performed on 16-lead Small Outline Integrated Circuit (SOIC) double batwing package mounted on a PCB. Several thermal enhancement features as well as the new package are modeled in the analysis. The results show that the indented leadframe package compares favorably with the heat slug enhanced SOIC package in thermal performance.

Key words:

Leadframe, Plastic Package, Thermal Enhancement, Thermal Analysis, and Thermal Optimization.

1. Introduction

More than ever before, small feature size electronic circuits have evolved into more circuit components and higher power dissipation per unit chip area and higher operating speed. The risk is a circuit die that is too hot to cool sufficiently. Concurrently, the demands for compact packaging, small package-to-die ratio, high input/output (I/O) counts, and light weight package continue to rise. Still, engineers are expected to come up with package designs to cope with these two conflicting trends. To make the required thermal design even more challenging, the electronics industry is heading toward a cost effective approach with small product footprint and chassis space. In all this, the plastic package continues to be the low cost choice[1]. To keep the operating temperature of such packaged devices under control for acceptable reliability and longevity, engineers search for all possible improvements in both package materials and design techniques.

A number of package and Printed Circuit Board (PCB) thermal enhancement features have been studied and discussed in this work[2,3]. Over the past several years, specific studies have been conducted on the effects of high thermal conductivity molding compound[4,5], heat spreader[6], heat slug[7], and PCB thermal conductivity[8]. Several improved leadframe designs have also been reported[9-11]. Since the package is mechanically and thermally coupled to the PCB, a complete thermal analysis requires the package and the PCB be considered as a unit. A PCB of poor thermal design is likely to become the bottle neck in restricting the heat removal capability of a high thermal performing package. The authors have

recently carried out the thermal analysis of a reference model consisting of a basic package and a basic PCB configuration[12,13]. Most recently, thermal enhancement features at both package and PCB levels were added to the reference model. The enhanced models were analyzed in detail to determine the thermal impacts of these features[14].

This study supports earlier findings that the majority of heat in a conventional plastic package is transported through its leads into the PCB[13]. In most packages, there is a significant temperature drop from the die-pad region of the leadframe to the lead pads on the PCB. Ideally, this thermal path should be as short as possible. To minimize this path, the researchers address the problem at its root, namely, the leadframe design. After several iterations, a new package is proposed. The unique feature of the new leadframe design is that the die-pad region is indented to expose its bottom surface to the package exterior. The die-pad region is suspended and supported by four corner tabs. The bottom surface of the die-pad region is nearly flush with the bottom surface of the plastic molding. In this paper, the authors first review the thermal performance of the reference model for comparison purpose. The model with thermal slug in the package attached to the PCB is also presented for comparison. The new package with indented leadframe is then presented with its thermal performance and advantages discussed. Distributions of heat to leads and thermal enhancement features are elaborated in this publication.

2. Reference Package and Printed Circuit Board

As a preliminary study, a basic reference model is constructed using Finite Element (FE) tools[15]. The basic model consists of a plastic package mounted on a PCB. The thermal performances after incorporation of each thermal enhancement feature are analyzed using the basic model as a reference. Figure 1 displays the basic package mounted on the basic PCB. The package leads are attached to the PCB pads by a layer of 50μm lead-tin solder with thermal conductivity of 0.49W/cm° C. The basic package is a 16-lead SOIC plastic package. The temperature contour shows the surface temperature of the structure. The package consists of four major layers with its physical dimensions and properties listed in Table 1. To take

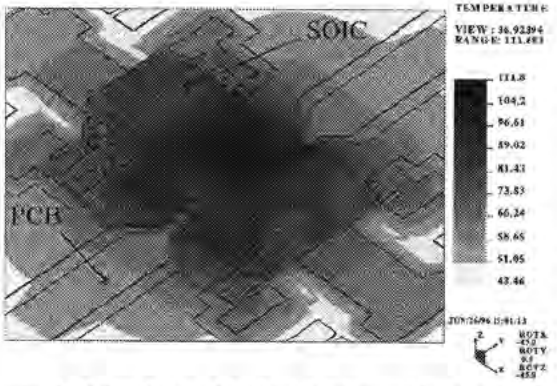


Figure 1. Detailed view of the basic package soldered on the basic PCB.

Table 1. Physical properties of the package.

Layer Number	Material	Thickness (cm)	Thermal Conductivity (W/cm°C)
1	Molding compound	450	7.0×10^{-3}
2	GaAs	125	045 @ 27°C
3	Copper leadframe	200	3.6
4	Molding compound	650	7.0×10^{-3}

into consideration the cooling effect of surrounding air, a free air convection coefficient of 1×10^{-3} W/cm^2 °C is prescribed on all surfaces of the entire package and the PCB. The ambient temperature is specified at 27°C. The convective heat is given by $Q = hA(T_s - T_a)$, where Q is the power in Watt, h is the convection heat transfer coefficient, A is the convection area, T_s is the temperature on the convective surface, T_a is the ambient temperature.

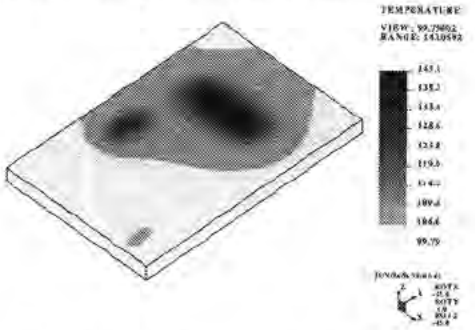


Figure 2. GaAs die with temperature contour.

Figure 2 exhibits the temperature contour on the surface of the die that is located inside the plastic package. The dimension of the die is 1980μm x 1300μm with a thickness of 125μm. The die contains three heat generating field effect transistors (FETs) of 610μm x 230μm dissipating 1.61 W, 300μm x 75μm dissipating 0.41W, and 125μm x 1μm dissipating 0.06W. The researchers can observe that the temperature distribution on the die surface is very nonuniform, giving rise to a temperature drop of 43.3°C from the hottest spot to the coldest region. This large temperature gradient is due to the concentrated heat sources. In the die model, the temperature dependence of GaAs thermal conductivity is taken into account. Figure 3 portrays the double batwing leadframe of the basic package. The leadframe is modeled in details to reflect the actual geometry. Notice that the ground leads are the batwing leads extending from the die pad area. From the Finite Element results,

it is calculated that the ground leads transport 74.3% of the heat out of the basic plastic package. This characteristic indicates the importance of vias in the PCB for ground leads.

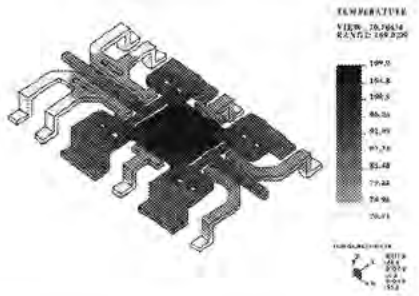


Figure 3. Copper leadframe with temperature contour.

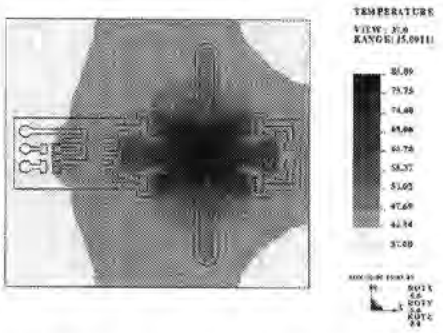


Figure 4. Top view of the reference PCB showing the detail copper traces with temperature contour.

Figure 4 exhibits the top view of the complete PCB model with temperature contour. It is a 42mm x 38mm four-layer 1-oz copper PCB with a total thickness of 1.6mm. The physical properties of the PCB are listed in Table 2. The PCB surfaces are prescribed with an air convection coefficient of 1.0×10^{-3} W/cm^2 °C. The ambient temperature is set at 27°C. To emulate the condition at use, it is assumed that four corners of the PCB are mounted on a chassis with an isothermal temperature of 37°C. The mounting holes are plated through the PCB to form the thermal vias. Near the right edge, the back side of the PCB has a stripe of copper mounted to a bracket at 37°C. All vias are modeled as via filled with lead-tin solder having a thermal conductivity of 0.49W/cm°C. Layer 1 is the component side with copper trace covering about 85% of the PCB area. The copper traces are modeled in details as seen in Figure 4. Layer 3 is the first inner copper plane used as ground layer. Layer 5 is the second inner copper plane used for power supply. Layer 7 is used as a ground plane again. All these three layers have nearly 100% copper coverage except at the via hole cutout for signal and power distributions or planes. The complete FE model including package and PCB consists of 28,228 elements and 32,241 nodes.

Table 2. Physical properties of the PCB.

Layer	Material	Thickness (cm)	Thermal Conductivity (W/cm °C)
1	Copper	36	3.6
2	FR-4	478	1.8×10^{-3}
3	Copper	36	3.6
4	FR-4	478	1.8×10^{-3}
5	Copper	36	3.6
6	FR-4	478	1.8×10^{-3}
7	Copper	36	3.6

3. Thermal Enhancement Features

Thermal enhancement can be applied to both the package and the PCB to improve the thermal performance of the entire structure. The enhancement technique sometimes is chosen based upon experience. However, every combination of die, package, and PCB has its own characteristics that cannot be duplicated exactly from others. Thus, a complete analysis of a package mounted on a PCB may be needed to ensure an optimum choice. Possible thermal enhancements include improved thermal conductivities for molding compound[4] and PCB[7], thicker copper on PCB[3], fused and batwing leadframes, thermal via, heat spreader[5], and heat slug[3,6]. To investigate the optimal thermal path from the die to the PCB, the researchers first analyze the features of lead vias in the PCB and heat slug on the package. From the results, they came up with an indented leadframe design to be presented in the next section. This design offers the shortest possible thermal path from the die to the PCB level.

The first enhancement feature analyzed is the PCB via that is connected to the ground lead. It is one of the simplest and most economical thermal enhancements. Not only does it provide the electrical connection between different copper layers, it also diverts heat into all copper layers. Thus, it increases heat conduction into the nearby isothermal boundaries. The thermal advantage of the lead via is well justified for its minimal extra steps in manufacturing. To accomplish the most effective heat removal, lead vias should be located underneath the leads that have short thermal path from the die, such as the ground leads. These vias help the heat spread into all copper layers quickly. The holes for mounting the PCB should also be made as lead vias and locate close to the components that dissipate most of the power. Since mounting holes are usually connected to the chassis with nearly isothermal temperature, the heat
can be sunk with the shortest thermal path. With four 1-mm diameter vias right below the batwing ground leads of the SOIC package, the peak temperature on the die decreases from 143.1°C to 119.5°C, a reduction of 23.6°C, as shown in Table 3. Among this reduction, 21.2°C occurs in the PCB as a result of the four lead vias, consistent with the physical argument.

The second enhancement feature studied is the heat slug attached to the package. It is a metal piece usually made of copper with one side attached to the die-pad region of the leadframe and the opposite side exposed on the package surface. It can carry heat directly from the die through the die pad to the package surface provided that the surface is properly sunk. A heat slug could be an excellent thermal enhancement. However, improper usage and inadequate PCB design usually depress the full potential of the heat slug. For example, a heat-slugged package without the slug attached to the PCB utilizes little of its capability. In this case, the slug functions only as a heat spreader rather than as a heat conduction channel, thus defeating its intended purpose. To exploit the full potential of a heat slug, it must be soldered to the PCB for direct heat conduction from the die to the PCB.

Table 3. Temperatures in °C at key locations.

Configuration	Die Peak Temperature	Hottest Die-Pad	Hottest Lead	Hottest PCB
1. Basic package on basic PCB	143.1	109.0	85.4	85.1
2. Basic package on PCB with lead vias	119.5	87.9	64.0	63.9
3. Package with heat slug on PCB with lead vias[1]	109.5	78.6	62.2	74.3
4. Package with heat slug on PCB with package via[2] and lead vias	104.0	73.9	60.3	68.3
5. Package with indented leadframe on PCB with lead and package vias	103.7	73.3	60.6	69.7

Note. The isothermal boundaries on PCB are set at 37°C and the ambient temperature is 27°C. (1) Lead vias are plated through holes on printed circuit board connecting either ground or power copper layers. (2) Package via is a thermal via located underneath the heat slug or indented leadframe connecting the package to the ground copper layers.

Figure 5 exhibits the temperature contour of the model with a 1.9mm x 1.2mm x 0.7mm copper heat_slug underneath the leadframe.

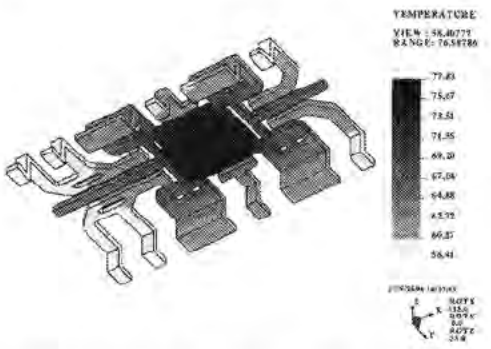


Figure 5. The model with the 1.9mm x 1.2mm x 0.7mm copper heat slug. The slug is joined right underneath the middle of the leadframe.

The slug has thermal conductivity of 3.6W/cm°C. The slug bottom surface is soldered to the ground plane on the PCB by a 150-μm layer of lead-tin solder having thermal conductivity of 0.49W/cm°C. With the four lead vias underneath the ground leads still in place, the slug enhancement further brings down the die peak temperature to 109.5°C, shown in Table 3. The slug alone draws 31.64% of the total power from the die into the PCB. To improve the thermal performance of the package further, a package via with a diameter of 1.2mm is added in the PCB underneath the center of the slug. This package via spreads heat even more to the copper layers, thus lowering the die peak temperature to 104.0°C.

To clearly observe the effects of the enhancements, temperatures at key locations in the structures are compiled in Table 3. Results of the indented leadframe design are also included. This design will be presented in the next section. From the die peak temperature column, it is seen that the effect of the four lead vias underneath the ground leads is very significant. This simple enhancement in the PCB reduces the peak temperature to 119.5°C, a reduction as much as 23.6°C. With additional heat slug enhancement in the package, the peak temperature further decreases by another 10.0°C, yielding 109.5°C. Since the heat slug carries 31.64% of the total power from the die as will be shown in Table 5, a package via located underneath the slug brings the peak temperature down to 104.0°C, giving a 5.5°C improvement over the case with slug but no package via in the PCB.

4. The Package with Indented Leadframe

The large majority of heat in a conventional plastic package is transported through its leads into the PCB. In most packages, there is significant temperature drops from the die-pad region of the leadframe to the lead pads on PCB. The heat slug enhancement feature presented in Section 3 greatly reduces this thermal path by providing a direct conduction path from the leadframe die pad region to the PCB. Ideally, this thermal path should be as small as possible. To minimize this thermal path, one can investigate the problem at its root, such as the leadframe design. After several iterations, an indented leadframe design is finally obtained. The unique feature of the new design is that the die-pad region is indented to expose its bottom surface to the package exterior. To compare this new design with the existing packages, an indented die-pad leadframe design having the same footprint as a 16-lead SOIC double batwing package is modeled. Figure 6 portrays half of the resulting leadframe. The die-pad region is suspended and

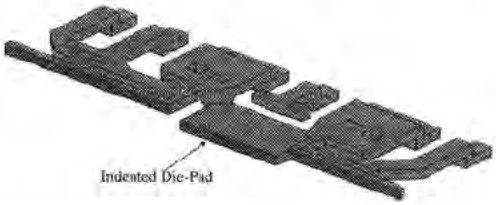


Figure 6. Half of the indented leadframe.

supported by four corner tabs. The bottom surface of the die-pad region is nearly flush with the bottom surface of the plastic molding. Table 4 shows the layers and physical properties of the new package. The total package thickness is about 0.71mm. In the model, the bottom surface of the indented die-pad region is joined by a 150-μm solder layer to the PCB that is described in Section 2. The package via in the PCB has dimension of 1.1mm x 1.1mm and it is located right underneath the center of the die-pad region.

Table 4. Physical properties of the package with indented leadframe.

Layer number	Material	Thickness (μm)	Thermal conductivity (W/cm°C)
1	Molding compound	250 (a) 360 (b)	7.0×10^{-3}
2	GaAs	125	0.45 @ 27°C
3	Copper leadframe	200	3.6
4	Molding compound	250 (a) 0 (b)	7.0×10^{-3}

Note (a) at un-indented area (b) at indented area

Figure 7 displays the indented leadframe of the new package with temperature contour. Calculated temperatures at key locations are shown in Table 3. The die peak temperature of the new package, configuration number 5, is 0.3°C lower than that of the slug enhanced model, configuration number 4. The temperature drop from the peak temperature location on the die to the hottest PCB location, ΔT_{DB}, is 35.7°C for the slug enhanced model and 34.0°C for the indented leadframe package. Since the hottest PCB location is right underneath the solder layer that mounts the packages, it

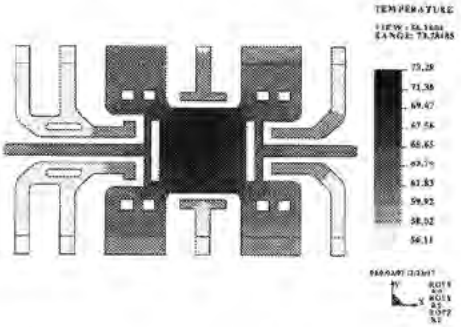


Figure 7. Temperature contour on the indented leadframe of the new package.

is clear that the new package achieves significantly shorter thermal path from the die to the PCB. Accordingly, the package with indented leadframe compares favorably with the slug enhanced package in terms of thermal performance. In addition, this new package has the following potential advantages,

1. The exposed die-pad surface can be soldered to a thermal via in the PCB, providing the shortest possible thermal path from the die to the PCB to accomplish the best thermal performance.
2. The additional solder joint that connects the exposed die-pad to the PCB, greatly enhances the mechanical strength of the package mounted onto the PCB, thus increasing the reliability of the PCB assembly.
3. Since the die top surface is almost in plane with the bonding pads on the leadframe, the wire bonding process is easier and the wire can be shortened to reduce the inductance value.
4. Since the bottom surface of the indented die-pad region is soldered onto the PCB, it serves as the best possible electrical ground.

Items 3 and 4 above are particularly important for RF and microwave devices.

In assembly, the exposed die-pad region is mounted in the same soldering operation as the leads. Thus, the additional cost required for the above performance improvements results from a few extra stamping steps for the die-pad indentation. It is thus concluded that the new package design can be implemented at low cost compared to other thermal enhancement features. One concern of the new package is that only one side on the indented portion of the leadframe has molding compound. It is suspected that this asymmetrical geometry may cause warping. However, the molding compound is only 250μm in thickness, one can speculate that the 200μm thick leadframe would have enough strength to stay flat. Alternatively, a molding compound with thermal expansion coefficient close to copper can be used to reduce possible warping. In actual product design, the designer is expected to carry out mechanical modeling to simulate the bending of the structure. Mechanical modeling is not performed in this paper as it is beyond the scope of this work.

5. Discussion of Modeling Results

From Table 3, it shows that the temperature drops from the junction to the hottest die-pad location are quite similar for the various configurations. The reference model has the largest temperature drop from the junction to the die-pad, that is 34.1°C. This is caused mainly by the temperature dependence of GaAs thermal conductivity, such as higher temperature results in lower GaAs thermal conductivity. Since nearly all heat is conducted through the die and the die-pad as shown in Table 5, it is reasonable to conclude that the

Table 5. Heat flow distribution of the package for all five configurations.

Pin #	Reference Model	Lead Vias	Slug without Package Via	Slug with Package Via	Indented Leadframe
1	2.13%	1.06%	0.88%	0.72%	0.63%
2	2.60%	0.96%	0.78%	0.65%	0.53%
3&4(ground)	17.94%	20.47%	13.36%	10.10%	8.08%
5	3.83%	2.23%	1.76%	1.42%	1.14%
6&7(ground)	18.20%	21.21%	14.29%	10.82%	8.56%
8	2.89%	1.39%	1.16%	0.95%	0.83%
9	2.92%	1.40%	1.17%	0.96%	0.84%
10&11(ground)	19.19%	22.46%	14.81%	11.33%	9.10%
12	4.03%	2.42%	1.85%	1.51%	1.26%
13&14(ground)	18.91%	21.81%	13.94%	10.68%	8.78%
15	2.02%	0.97%	0.78%	0.63%	0.53%
16	2.15%	1.07%	0.88%	0.72%	0.63%
Package Convection	4.19%	2.89%	2.69%	2.51%	2.32%
Package Enhancement	N/A	N/A	31.64%	47.02%	56.77%

thermal resistance of the die itself does not differ much among the thermal enhancements incorporated beneath the die-pad region of the leadframe and in the PCB. The temperature drops between the hottest die-pad location and hottest lead are similar for the reference model and the lead via configuration since the leads are the only heat conduction path from the package into the PCB. However, for the configurations with heat slug and indented leadframe, a large amount of heat is shunted through the short thermal path provided by the slug or the indentation. As a consequence, less heat is conducted through the leads, resulting in reduction in the temperature drop from the die-pad to the hottest lead.

It is clear that different enhancement features give different thermal performance improvement. To further understand how the heat generated on the die flows through various transport paths, Table 5 is compiled to exhibit the power that is dissipated through each of the 16 package leads, the heat slug and the indented die-pad, and that convects through package surface by free air convection. The power is given in terms of percentage of the total power dissipated by the die. Thus, for each configuration, the sum should add up to 100%. Notice how the power drawn by the ground leads increases from the reference model to lead via configuration. Also, the power that conducts to non-fused leads and that convects through package surface decreases from the reference model to lead via configuration. In the sequence of configurations; the slug without package via, and with package via to that of indented leadframe, the heat conducted through non-fused leads, and convected through package surface progressively decreases, thus the power conducted through the ground leads. This can be attributed to the additional short and direct thermal path provided by the heat slug (31.6%), the heat slug with via (47.0%), and the indented die-pad (56.8%). The heat that conducts through the leads, the thermal slug, and the indented die-pad is discharged into the PCB. With respect to the PCB, 29.2% for the reference model convects through the PCB surfaces and the rest is sunk into the boundaries held at 37°C. For the other configurations, about 28% convects through the PCB surfaces and the rest is sunk into the boundaries.

6. Summary

This study supports previous findings that heat in a conventional package is mostly transported through its leads into the PCB. In most packages, there is a large temperature drop from the die-pad region of the leadframe to the PCB. Ideally, this temperature drop should be as small as possible. To minimize this thermal path, the authors examine the problem at its root, namely, the leadframe, and devise an indented leadframe design. The unique feature of the new design is that the die-pad region is indented to expose its bottom surface to the package exterior. The die-pad region is suspended and supported by four corner tabs. The bottom surface of the die-pad region is nearly flush with the bottom surface of the plastic molding. In assembly, the bottom surface is soldered to the PCB to provide the best possible thermal performance and electrical ground.

The indented leadframe design is realized with the same footprint as a 16-lead SOIC package having double batwing. To study the thermal performance of the new package, it is attached to a reference PCB. The complete assembly is modeled using Finite Element techniques. A conventional SOIC package with heat slug is also analyzed for comparison purpose. The results show that the new package performs favorably in comparison to the slug enhanced package. The new package design should find applications in high frequency and power electronic and optoelectronic devices.

References

1. Rao. R. Tummala, (Editor), Microelectronics Packaging Handbook, Van Nostrand Reinhold, New York, 1989.
2. D. Edward, M. Hwang, and B. Stearns, "Thermal Enhancement of Plastic IC Package," IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT, Vol. 18, pp. 57-67, March 1995.
3. B. Stearns, P.B. Simon, and M. Murtuza, "Performance Comparison of Thermally Enhanced Plastic (TEP) Packages," Proceedings of the Electronic Components and Technology Conference, ECTC '95, Las Vegas, Navada, pp. 1134-1139, May 21-24, 1995.
4. M. Michael and L. Nguyen, "Effect of Mold Compound Thermal Conductivity on IC Package Thermal Performance," Proceedings of the IEEE Intersociety Conference on Thermal Phenomena in Electronic Systems, Austin, Texas, pp. 246-252, February 5-8, 1992.
5. D. Tracy, et al., "Reliability of Aluminum Nitride-Filled Mold Compound," Proceedings of the Electronic Components and Technology Conference, ECTC '97, San Jose, California, pp. 72-77, May 18-21, 1997.
6. T. Moore, "The Design and Characterization of a High Thermal Efficiency Leadframe with an Integral Heatspreader," Proceedings of the IEEE Semiconductor Thermal Measurement and Management Symposium, Phoenix, Arizona, pp. 98-104, February 12-14, 1991.
7. B.M. Guenin, D. Mahulikar, D.C. Leslie and M. Holmes, "Reliability and Performance of Non-Hermetic, Surface Mount Quad Flat Packages," Proceeding of the Electronic Components and Technology Conference, ECTC '94, Washington, DC, pp. 721-727, May 1-4, 1994.
8. H. Shaukatullah and M.A. Gaynes, "Experimental Determination of the Effect of Printed Circuit Card Conductivity on the Thermal Performance of Surface Mount Electronic Packages," Proceedings of the IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, California, pp. 44-52. February 1-3, 1994.
9. S. Omi, T. Maruyama, T. Ishio, A. Narai, and Y. Sota, "Development of 0.45mm Thick Ultra-thin Small Outline Package," Proceedings of the Electronic Components and Technology Conference, ECTC '94, Washington, D.C., pp. 498-505, May 1-4, 1994.

10. K. B. Cha, Y. G. Kim, T. K. Kang, D. S. Kang, and S. D. Baek, "Ultra-thin and Crack-free Bottom leaded Plastic Package Design," Proceedings of the Electronic Components and Technology Conference, ECTC '95, Las Vegas, Nevada, pp. 224-228, May 21-24, 1995.
11. T. Moore, "Thermal Coastline - Leadframes for High Power at No Cost," Proceedings of the Electronic Components and Technology Conference, ECTC '97, San Jose, California, pp. 332-337, May 18-21, 1997.
12. Dave H. Chien, Chin C. Lee, Mike Rachlin, Andy Peake, and Thomas Kole, "Thermal Analysis and Measurement of Plastic Packaged GaAs Devices," Proceedings of the IEEE Semiconductor Thermal Measurement and Management Symposium, Austin, Texas, pp. 89-96, March 5-7, 1996.
13. Dave H. Chien, Chin C. Lee, Mike Rachlin, Andy Peake, and Thomas Kole, "Thermal Analysis of Packaged GaAs Devices Using Chip Model with Finite Element Method," International Journal of Microcircuits and Electronic Packaging, Vol. 20, No. 1, pp. 3-11, March 1997.
14. David H. Chien, "Thermal and Stress Modeling of Packaged Semiconductor Devices," Ph.D. Dissertation, University of California, Irvine, December 1996.
15. NISA Heat Transfer, Engineering Mechanic Research Corp., Michigan.

About the authors

Chin C. Lee was born in Taiwan. He received the B.E. and the M.S. Degrees in Electronics from the National Chiao-Tung University, Hsinchu, Taiwan, in 1970 and 1973, respectively, and the Ph.D. Degree in Electrical Engineering from Carnegie-Mellon University, Pittsburgh, Pennsylvania in 1979. From 1979 to 1980, he was a Research Associate with Carnegie-Mellon University. From 1980 to 1983, he was with the Electrical Engineering Department of the University of California, Irvine, as a Research Specialist. In 1984, he joined the same Department as an Assistant Professor and became Professor of Electrical and Computer Engineering in July 1994. He served as the Graduate Advisor of Electrical and Computer Engineering at UCI from 1990/91 to 93/94. His research interests include semiconductor devices, electronic packaging, bonding technology, thermal analysis and design of electronic devices, integrated optics and photonics, electromagnetic theory and wave, acoustics and acoustic microscopy. He has co-authored three book chapters and more than 120 papers in the subject areas mentioned above. Chin C. Lee is a Senior Member of IEEE, and a member of the International Society for Boundary Elements and Tau Beta Pi. He has served on the Scientific Advisory Committee of MICROSIM Conference. He is an Associate Editor of IEEE Transactions on Components, Packaging, and Manufacturing Technology (CPMT) in the technical areas of solders and soldering techniques, joining and bonding technology, integrated optical and photonic components, thermal analysis and design, photonic and optoelectronic packaging, acoustics and acoustic microscopy

David H. Chien received the B.S. Degree from the California State University, Los Angeles in 1991, and the M.S. and Ph.D. Degrees from the University of California, Irvine in 1992 and 1996, respectively. He is currently a senior member of technical staff at TRW Space & Electronic Group. His interests include thermal and packaging design of semiconductor devices. He is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi.

Professor Chen Tsai is a naturalized citizen of the U.S. He received his Ph.D. Degree in Electrical Engineering from Stanford University in 1965. He was with the Lockheed Palo Alto Research Labs as a Research Scientist for three and a half years before joining Carnegie-Mellon University as an Assistant Professor in 1969. In 1974, he was promoted to Professor and was awarded an Endowed Professorship in 1979. In 1980, he joined UC Irvine as a Professor of Electrical Engineering, served as Acting Department Chair from 1985-86, and was advanced to Professor, Above-Scale in 1991. He has published some 290 research papers and ten encyclopedia and book chapters. He was the editor and contributed three chapters to the first topical volume on Guided-Wave Acoustooptics, published by Springer-Verlag in 1990. This author's group at UC Irvine has conducted basic research on Guided-Wave Acoustooptics and Magnetooptics, and Acoustic Microscopy through the sponsorships of the UC MICRO/Industry program, the NSF, the NSA, the AROD, the AFOSR, and the ONR. Among the numerous awards and honors he has received are the Fellows of the IEEE, the OSA, the American Association for Advancement of Science (AAAS), the SPIE, and the Photonics Society of Chinese Americans, the IEEE Distinguished Lectureship Award, UC Irvine Faculty Senate Distinguished Research Lectureship Award, and the International Microoptics Award.

EXHIBIT 12

www.archive.org
415.561.6767
415.840-0391 e-fax

Internet Archive
300 Funston Avenue
San Francisco, CA 94118

AFFIDAVIT OF CHRISTOPHER BUTLER

1. I am the Office Manager at the Internet Archive, located in San Francisco, California. I make this declaration of my own personal knowledge.

2. The Internet Archive is a website that provides access to a digital library of Internet sites and other cultural artifacts in digital form. Like a paper library, we provide free access to researchers, historians, scholars, and the general public. The Internet Archive has partnered with and receives support from various institutions, including the Library of Congress.

3. The Internet Archive has created a service known as the Wayback Machine. The Wayback Machine makes it possible to surf more than 450 billion pages stored in the Internet Archive's web archive. Visitors to the Wayback Machine can search archives by URL (i.e., a website address). If archived records for a URL are available, the visitor will be presented with a list of available dates. The visitor may select one of those dates, and then begin surfing on an archived version of the Web. The links on the archived files, when served by the Wayback Machine, point to other archived files (whether HTML pages or images). If a visitor clicks on a link on an archived page, the Wayback Machine will serve the archived file with the closest available date to the page upon which the link appeared and was clicked.

4. The archived data made viewable and browseable by the Wayback Machine is compiled using software programs known as crawlers, which surf the Web and automatically store copies of web files, preserving these files as they exist at the point of time of capture.

5. The Internet Archive assigns a URL on its site to the archived files in the format http://web.archive.org/web/[Year in yyyy][Month in mm][Day in dd][Time code in hh:mm:ss]/[Archived URL]. Thus, the Internet Archive URL http://web.archive.org/web/19970126045828/http://www.archive.org/ would be the URL for the record of the Internet Archive home page HTML file (http://www.archive.org/) archived on January 26, 1997 at 4:58 a.m. and 28 seconds (1997/01/26 at 04:58:28). A web browser may be set such that a printout from it will display the URL of a web page in the printout's footer. The date assigned by the Internet Archive applies to the HTML file but not to image files linked therein. Thus images that appear on a page may not have been archived on the same date as the HTML file. Likewise, if a website is designed with "frames," the date assigned by the Internet Archive applies to the frameset as a whole, and not the individual pages within each frame.

6. Attached hereto as Exhibit A are true and accurate copies of printouts of the Internet Archive's records of the HTML files or PDF files for the URLs and the dates specified in the footer of the printout (HTML) or attached coversheet (PDF).

7. I declare under penalty of perjury that the foregoing is true and correct.

DATE: 2/20/19

Christopher Butler

CALIFORNIA JURAT

See Attached Document.

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California
County of San Francisco

Subscribed and sworn to (or affirmed) before me on this

20th day of February, 2018, by

Christopher Butler,

proved to me on the basis of satisfactory evidence to be the person who appeared before me.

LAUREL KARR
Notary Public - California
San Francisco County
Commission # 2172222
My Comm. Expires Nov 17, 2020

Signature: Laurel Karr

Exhibit A

http://web.archive.org/web/20030606000026/http://allegromicro.com:80/selguide/pdf/hiperf.pdf

APPLICATIONS INFORMATION

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

ABSTRACT

A new, high-performance version of a Plastic Dual-In-Line package with improved reliability levels has been developed for high-power integrated circuit industrial and automotive applications. Superior thermal capability and reliability performances have been achieved with no increase in manufacturing cost or change in package outline.

The development of this package is based on a package optimization approach. Development methodology and package characterization results will be outlined. Data for production lots of the package show a thermal performance improvement of up to 35 percent compared with currently available packages, without the aid of an external heat sink. Furthermore, qualification test results indicate that this new package has an excellent reliability performance and its long-term survival exceeds the industry standard requirements. An improvement by a factor of 4 in the resistance to device metal deformation and a factor of 7 in wire-bond thermal fatigue has been achieved as a result of reducing the shear and normal stresses inside the package by proper selection of a state-of-the-art low modulus molding compound and optimizing the leadframe design. In addition, new design fundamentals will be briefly discussed.

This paper was presented at the 39th Electronic Components Conference, Houston, TX, May 22-24, 1989.

INTRODUCTION

As the maturation of power integrated circuit technologies continues to promise more miniaturization of power electronic systems, the role of package thermal management is becoming critical. Since the present power packaging technology lags sharply behind the chip technology, the device performance and its reliable operation can be described to a great extent as limited by the package thermal capability. This paper presents the results of a package design study, which employs a "package optimization approach." The package chosen for this study is the 16-lead web-DIP, class of Plastic Dual-In-Line-Package (PDIP), which was specifically developed for medium- to high-power applications. An important practical feature of the web-DIP is that it costs no more to produce than a conventional DIP.

The initial phase of this program is a comparative analysis, based on package thermal and physical evaluations. Five variations of power DIP packages from major power integrated circuit manufacturers were evaluated. The evaluation results indicate that packages presently available are still far from optimum, thus making further improvements a feasible goal. In parallel to the comparative analysis, three-dimensional finite-element models are constructed to simulate and analyze the expected thermal performance of the design under study. The projected configuration is also analyzed thermostructurally to examine the mechanical behavior of the new packaging system, prior to implementation. The reliability improvement of the new package is based on optimization of the leadframe design, and the proper selection of materials. The package reliability design is aimed at improving wire fatigue life and device metal deformation resistance during temperature cycling. In addition, the study provides a new insight into this type of package and new design principles that can be extended to packages of similar internal configuration, such as power surface-mount packages.

OPTIMIZATION STRATEGY

PDIP's are still the most common package option for high-volume IC production, due to their established manufacturing and handling, and their low cost. However, there are two different types of PDIP's. The first is the standard type in which the chip pad is not attached to any of the internal leads (Fig. 1(a)), and which is mainly used for low-power applications. The second is a modified form of the standard type in which the central leads are tied in pairs and connected with the paddle, forming one piece (Fig. 1(b)). This unconventional configuration has been employed to improve the package thermal performance, mainly by enhancing the conduction heat transfer mechanisms by

allowing the chip to be cooled directly by means of these four leads which are soldered to a board. This design format has made such a package suitable for medium-power applications up to 2.5 W in natural convection. Also, if the chip pad is extended to the outside of the package forming a web shape (Figure 1(c)), a miniature heat sink can be soldered to the web for even higher power dissipation.

WEB-DIP DESIGN

Although there are several extensive studies concerning thermal performance and reliability of standard PDIP's [1]-[4], there have been no similar efforts directed towards its web version. However, we felt that a new insight should be gained and established for the web-type package for the following reasons:

(1) The power dissipation capability of the package is greatly influenced by the web concept, which dramatically changes the temperature fields inside the package. Consequently, all of the previously identified thermal paths for standard packages are affected, and their relative thermal contributions are altered.

(2) It has been demonstrated that converting from the standard package to the web-type package has led to an improvement of the package power handling capability by 70 percent. For example, a 1-W standard package can dissipate 1.7 W instead by tying its four central leads to the chip pad. However, our observations, as will be described later, indicate that some package designers have conflicting views about the thermal merits of the concept compared with other paths. This limited understanding as to the precise relationship between the web and other leadframe parameters has cost some manufacturers a great thermal penalty, as will be explained in the next section.

(3) The mechanical configuration of the leadframe and its physical behavior within the package during assembly, testing, and

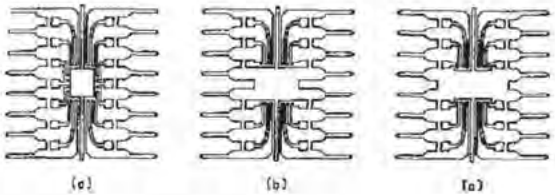


FIGURE 1
16-Lead PDIP leadframes (a) standard (b) unconventional (c) unconventional-web

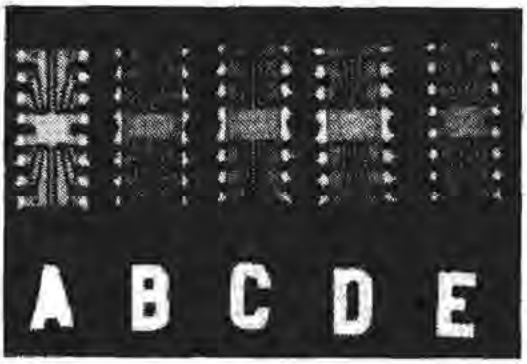


FIGURE 2
Leadframe designs for five different PDIP manufacturers

operation has introduced a considerable amount of uncertainty involving the package component structural responses and long- term reliability.

(4) Since this concept is being extended to new package families, notably PLCCs and SOICs, to improve their thermal performance, new safe design limits are required, particularly when these packages have not been completely perfected.

COMPARATIVE ANALYSIS

The primary purpose of this analysis was to assess the thermal performance of the industry state-of-the-art power DIP packages made by leading IC manufacturers. This performance evaluation enabled us to gain knowledge about the range of the thermal capabilities of existing packages and to establish an optimization target. Figure 2 shows the leadframe design of the examined packages.

Representative packages from five major companies including our targeted package were chosen for this study based on device perfor-

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

TABLE I

16-LEAD DIP THERMAL RESISTANCE R_{qJA} (°C/W)

Manufacturer	$R_{\theta JA}$ (°C/W) at 150°C T_J
A	47
B	51.5
C	52
D	55
E	59

mance equivalents and similarity of package outlines

Steady-state thermal resistance of the packages was measured in still air under the same conditions at different power levels, using the Temperature Sensitive Parameters (TSP) method. During the measurements, packages were mounted individually by soldering to a printed circuit board that was oriented vertically and housed in a 1-ft.^{3} plexiglas sealed enclosure. Measurements were taken with the aid of a Sage model Theta 400A thermal resistance tester. Results of the measurements of the thermal resistance from junction to ambient, $R_{\theta JA}$ are presented in Table I. The manufacturers are listed in ascending rank, based on their package performances.

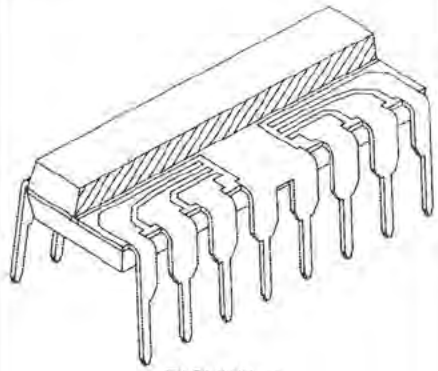


FIGURE 3

Web 16-lead PDIP

The next step of the analysis was to correlate these thermal resistances to their packaging systems. For this purpose, a construction analysis was performed. The results of the construction examination are summarized in Table II. The material analysis has been performed with the aid of a SEM equipped with an EDAX analyzer. Although it is not the intent of this study to critique these packages, the following discussion is in order.

WORST PERFORMANCE

Manufacturer E, whose package shows the highest thermal resistance, uses a very high thermal conductivity leadframe material which is identified as "silver-bearing copper." Its conductivity is 35 percent higher than that of Copper Alloy C194, used by other manufacturers. One might therefore expect that the package thermal resistance, $R_{\theta JA}$, would be lower than that of other packages employing C194 leadframes. However, as is indicated in Table I, this is not the case. The main reason is that the leadframe design has left out the tie bar. As a result, a dramatic increase in $R_{\theta JA}$ occurs, which is not compensated for by the higher conductivity leadframe. To verify this, an experiment was run with packages assembled using copper alloy C151 leadframes, whose conductivity is 25 percent higher than that of C194 leadframes. The tie bar was removed from some of these packages. Thermal resistance measurements showed that in natural convection cooling the leadframe material and the tie bar make separate contributions to $R_{\theta JA}$. First, despite the substitution of C194 material by C151, only about a 2.5°C/W improvement in $R_{\theta JA}$ is gained. The reason for this is that the package external resistance, $R_{\theta CA}$ (where C refers to both the package and lead surfaces) is the pre-dominant resistance, and is more than 75 percent of the package total resistance in still air. This $R_{\theta CA}$ has less dependency on the leadframe material [4], and is mainly a function of the motion and temperature of the boundary layers that exist on the package and the external lead surfaces. Second, packages with tie bar show a 6°C/W improvement in $R_{\theta JA}$ over packages assembled without a tie bar. Therefore, we conclude that the leadframe thermal conductivity has a minor effect on $R_{\theta JA}$, while the tie bar has a greater influence. This is due to its multiplying effect on heat distribution within the package to the adjacent leads as well as heat spreading to both the top and bottom surfaces of the packages, resulting in an additive thermal enhancement by conduction and convection. The same effect was also verified analytically, as will be discussed later.

BEST PERFORMANCE

Manufacturer A, whose package exhibits the lowest thermal resistance shown in Table I, employed the same high-conductivity leadframe material used by manufacturer E, but did not remove the tie bar. In addition, manufacturer A increased the leadframe thickness to 15 mils from the standard 10 mils. To evaluate the impact of the leadframe thickness on the package power handling capability, packages assembled with C194 and C151 leadframes with 10-, 12-, and 15-mil thickness were evaluated. Results of thermal resistance mea-

TABLE II
16-LEAD DIP CONSTRUCTION ANALYSIS

Manufacturer	Leadframe Material	Leadframe Thickness (mm)	Chip Thickness (mm)	Die-Attach Material	Gold Wire Diameter (mm)	Leadframe Design (Refer to Fig. 1)
A	Silver-Bearing Copper	0.375	0.250	Solder	0.0375	(b)
B	Copper Alloy C-194	0.250	0.350	Silver Epoxy	0.0375	(c)
C	Copper Alloy C-194	0.250	0.450	Silver Epoxy	0.0375	(c)
D	Copper Alloy C-194	0.250	0.250	Silver Epoxy	0.375	(c)
E	Silver-Bearing Copper	0.250	0.350	Silver Epoxy	0.325	(b)

surements in still air are summarized as follows:

(1) $R_{\theta JA}$ for packages assembled with 10-mil C151 leadframes was 2.5°C/W lower than those assembled with 10-mil C194 leadframes.

(2) Packages assembled with 12- and 15-mil C151 leadframes showed an improvement in their $R_{\theta JA}$ by 3.5 and 7°C/W respectively over packages with 10-mil C151 leadframes.

Thus it is concluded that a thicker leadframe reduces the package heat spreading resistance and enhances the package surface thermal properties that result in improved thermal exchange between the package surfaces and their immediate surrounding air layers. As a result, $R_{\theta CA}$ is also reduced.

THERMAL MODELING

FINITE ELEMENT PROGRAM

In parallel to the comparative analysis, numerical solutions for a steady-state thermal model were obtained by using the finite element program, ANSYS. A three-dimensional (3-D) model for a typical web-16-lead package was first constructed as a reference model to simulate the thermal performance of a standard web-16-lead DIP for a typical package system. Parametric changes were then applied to the model to determine the best variable combinations which can be implemented to optimize the package power dissipation, while maintaining a constant junction temperature of 150°C. Major variables investigated in this study were:

1 - leadframe material
2 - leadframe thickness
3 - tie bar size and layout
4 - lead lock hole size
5 - leadframe design, (web design versus internal termination), see Figures 1(b) and (c)
6 - die attach material
7 - die pad area

MODELING PROCEDURES

A typical web-DIP is shown schematically in Figure 3. Due to symmetry, only half of the package was modeled, with an adiabatic boundary condition at the symmetry plane. The model consists of 3032 nodes and 2270 elements. A 3-D view of the model is shown in Figure 4. A steady-state thermal analysis with free convection cooling is assumed. For half of the package, a 1.2-W dissipated power was used to simulate a 150°C junction temperature. The power was assumed to be uniformly generated in a 0.025-mm-thick active layer at the top of the silicon chip. For half of the chip (1.5 mm x 3.38 mm), the power was specified as heat generation per unit volume (9.49 W/mm³). The surfaces of the package and the external leads were assumed to have a convective heat transfer coefficient of 0.00001 W/mm²°C. Table III shows the materials properties that were used in the analysis.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-ICs

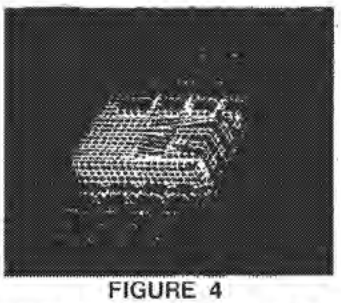


FIGURE 4

16-Lead DIP finite element model (3-D view)

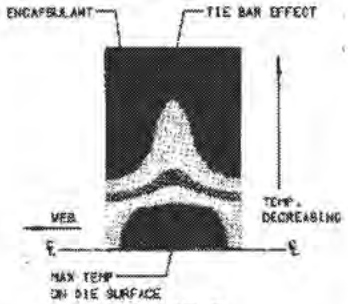


FIGURE 5

Temperature distribution on the die surface

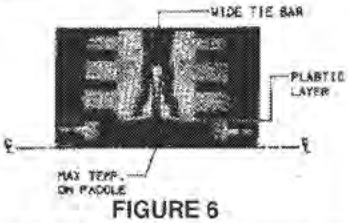


FIGURE 6

Temperature distribution across the leadframe surface

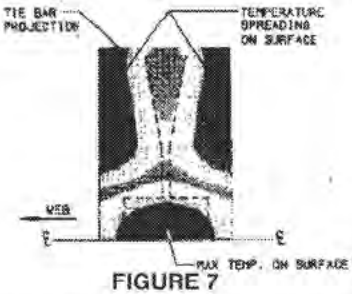


FIGURE 7

Temperature distribution on the package top surface

MODELING RESULTS AND DISCUSSION

Reference Model: The temperature distribution across the chip active layer is shown in Figure 5. The individual roles of the web and the tie bar in the package thermal performance are illustrated in Figure 6. It can be seen from Figure 6 that the web represents the primary thermal path in the transverse direction to the chip, where heat is directly conducted down through the chip pad out of the package to the connected protruding leads and dissipated into the board by conduction and to the air by convection and radiation. Also, it can be seen that the major remaining thermal barrier inside the package is the plastic layer between the chip edge and the lead tips, while the tie bar has a multiplying effect in dissipating and spreading heat to the adjacent leads and top and bottom surfaces of the package, as illustrated in Figures 6 and 7. Therefore, to achieve an effective thermal design, the plastic layer should be minimized and a massive tie bar utilized.

Parametric Study: For this analysis, the power generated in the active layer is held fixed and the junction temperature allowed to vary while variables are applied. The results and conclusions of this parametric study are summarized as follows: (i) In natural convection cooling, for high-conductivity leadframe material, $R_{\theta JA}$ has a minor dependency on the material thermal conductivity. An increase in thermal conductivity of 25 percent yields an 8 percent decrease in $R_{\theta JA}$. The leadframe thickness is of somewhat greater influence, yielding a 10 percent decrease in $R_{\theta JA}$ for only a 20 percent increase in thickness. Both $R_{\theta JC}$ and $R_{\theta CA}$ are decreased, due to the massive size of the thicker frame and its effect of reducing the package internal resistance and improving the convection mechanism. (ii) The tie bar is critical to the package thermal performance even in the presence of the web feature because of its contribution in directing the heat flow throughout the package and disseminating heat to the package surfaces. Therefore, the package designer should not be tempted to remove it from the leadframe. (iii) Extending the chip pad outside the package has a thermal contribution. A 1.6°C/W increase in $R_{\theta JA}$ was found when the web had been removed and the paddle was terminated inside the package as in the case of package type in Figure 1 (b). (iv) Lead lock holes of 0.2 mm² each have no effect on the package thermal performance if they are placed on all the leads except the four central leads. (v) An improvement in $R_{\theta JA}$ of only 1.2°C/W was achieved by changing the die-attach material from epoxy to solder, despite the large difference in their conductivities. This is attributed to the very small thickness of this layer. (vi) For a given chip, $R_{\theta JA}$ is insensitive to the increase in the die pad area beyond a critical dimension, since any increase in the paddle area in the longitudinal direction is accompanied by moving the lead tips away from the chip edge which results in increasing the plastic thickness between the chip and the leads, thus, increasing lead resistance. Complete numerical data are summarized in Figure 8. The accuracy of these data is within 10 percent of the experimental results.

TABLE III

MATERIAL PROPERTIES OF 16 LEAD-PDIP PACKAGE COMPONENTS

Material	Thermal Conductivity (W/mm · °C)	Thermal Expansion Coefficient (10^{-6}/°C)	Poisson's Ratio	Young's Modulus (kg/mm²)
Molding compound	0.75×10^{-3}	19	0.30	1500
Leadframe, C194	0.263	17	0.30	12 300
Silicon	0.140	2.4	0.28	17 000
Epoxy adhesive	0.004	20	0.30	6000
Leadframe, C151	0.331	17	0.30	12 300
Solder die attach	0.025	29	0.35	1800

Based on these data, we have predicted that a potential improvement in the package thermal performance of 25 percent could be achieved over our targeted package. It is also estimated that the proposed package could achieve a 40 percent increase in power dissipation capability over the worst case. Consequently, we decided to develop a new leadframe to meet the absolute targeted thermal improvement with the following characteristics: (i) optimum configuration, (ii) higher thermal conductivity copper C151, and (iii) increased thickness, 0.375 mm compared to the standard 0.25 mm thickness. The reliability aspects of the new package are detailed in the reliability improvement and in the thermostructural modeling sections.

RELIABILITY IMPROVEMENT

Although the package thermal enhancement seems to be the principal driving force for this program, package reliability improvement has been an intrinsic part of the package optimization strategy. For example, two separate studies recommended the use of (i) a new epoxy die-attach adhesive for its effectiveness in reducing the amount of voids and improving the die shear resistance, and (ii) a new state-of-the-art low modulus molding compound which has proven its contribution in reducing the shear force on the die surface. Experimental results with the low-modulus molding compound showed a reduction in device metal deformation by a factor of 4, after temperature cycling from -65°C to 150°C. The low stress characteristics of this new molding compound result from lowering its Young's modulus, without sacrificing the glass transition temperature for the finished product. [5], [6].

MECHANISM OF GROUND WIRE BOND FATIGUE AND RELIEF

A novel leadframe design change has extended the fatigue life of grounding wires during temperature cycling by a factor of 7. Earlier temperature cycling tests had indicated the occurrence of a wedge bond (heel), failure of the grounding wire that is used for a large number of devices. The failure mode was identified as a rupture or fracture occurring at the heel of the bond located on the leadframe, particularly on the die pad periphery, as seen in Figure 9. Experimental observations indicated that the mechanism of the bond fatigue failure is plastic flow and rupture in the heel area induced by cumulative cyclic strain during thermal fluctuations. The identified failure mechanism can briefly be described as follows: (i) An excessive reduction in the heel cross-sectional area, accompanied by plastic deformation, is caused by the edge of the bonding tool. (ii) The bond knee, which represents the junction between the heel and the wire span, sustains high localized stress by virtue of stress concentration effects. (iii) This stress will be intensified by the superimposed molding stress. (iv) As the package undergoes temperature changes under temperature cycling conditions the heel is displaced. The displacement has both a horizontal and a vertical component. The horizontal component results from the shear force which is due to thermal coefficient mismatch between the molding compound and the leadframe, while the vertical component results from the molding compound normal stress. (v) Due to very low yield strength and high ductility of

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

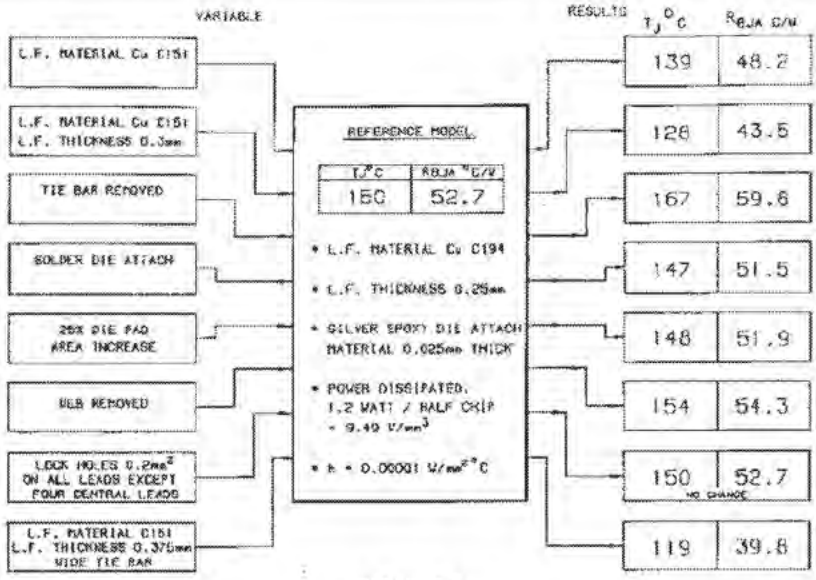


FIGURE 8

Numerical results of 3-D finite element analysis.

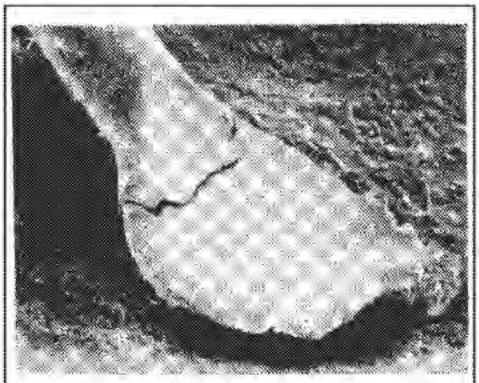


FIGURE 9

Wire heel damage after 1000 temperature cycles.

the gold wire, the displacement will produce a large amount of plastic strain, i.e., permanent deformation, at the knee for each temperature cycle. This plastic strain will accumulate during the course of the temperature cycling. (vi) In addition, during the high-temperature part of the cycle, a significant reduction in the gold yield strength could occur and the wire can behave as a perfectly plastic material [7] which will yield a very large cyclic strain at the knee and the molding compound interface. (vii) As the plastic straining continues and the cumulative magnitude of cyclic plastic strain reaches critical value (gold fracture strength), the heel will rupture at the knee and a fatigue crack can initiate, marking the beginning of the bond failure.

Analysis of experimental data suggested that the bond failure during temperature cycling is a function of heel strain. As a result, it was inferred that the bond fatigue life or number of cycles to failure can be expressed by the Coffin Law [8]

$$\Delta e_p = C/\sqrt{N}$$

where

Δe_p = cumulative plastic strain

N = number of cycles to failure

C = constant.

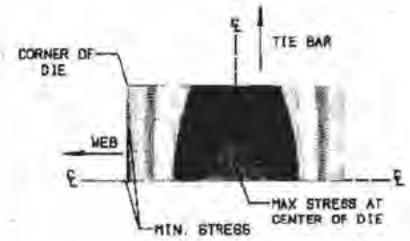


FIGURE 10

Die surface tensile stress distribution after die attach.

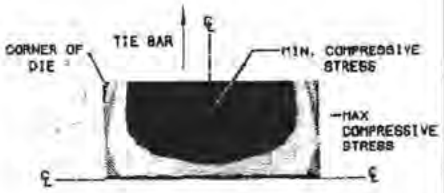


FIGURE 11

Die surface compressive stress distribution after die molding.

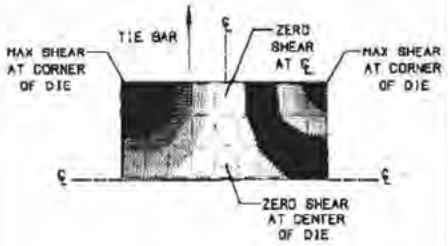


FIGURE 12

Die surface shear stress distribution after molding.

Consequently, to improve the bond fatigue life, the heel cumulative plastic strain should be minimized during temperature cycling. Based on the discussion outlined above, the leadframe was designed to satisfy the plastic strain-number of cycles to failure criterion. The new leadframe design concept for reducing the cyclic strain, and in turn improving the bond fatigue life, is based on the following mechanical approaches which have been substantiated by reliability data and experimental verifications.

(1) Decreasing the area of the heel supportive, underlying pad of the leadframe would reduce the plastic strain amplitude. This is due to the reduced effect of the thermal coefficient mismatch between the leadframe and the molding compound.

(2) Reduction in the heel displacement can be achieved by minimizing the heel pad movement. Therefore, an improvement of the interfacial adhesion between the heel and the surrounding will reduce the pad displacement. Consequently, stresses transmitted to the heel-molding compound interface will be reduced.

(3) The fatigue damage accumulation of the heel is not only dependent on pre-mold stress [9], but mostly on the plastic straining effects resulting from mechanical interaction between the molding compound and the configuration of the underlying pad.

THERMOSTRUCTURAL ANALYSIS

Although the proposed leadframe posed an attractive option to augment the package power dissipation capability, its mechanical compatibility with other package components was considered to be the key factor for its final utilization for long-term reliable performance. Therefore, a thermostructural analysis study was performed to compare the structural behavior of the new package system, with the thicker C151 leadframe, versus the standard package, whose leadframe thickness is only 0.25 mm. Since the new leadframe material, C151, and the standard leadframe, C194, have the same elastic moduli and coefficients of thermal expansion, the only variable considered in the analysis is the thickness (see Table III).

3-D FINITE ELEMENT MODELING

As the state of the shear and normal stresses on the die surface are of prime reliability concern, due to their role in device passivation cracking and metal deformation [10]-[12], they were analytically investigated after the die attach and molding processes. Only the web feature is considered, since the tie bar and other leads do not significantly affect the package system during these two processes. The following assumptions are made: (1) linear elastic analysis, (2) isotropic materials, (3) zero stress at or above the glass transition temperature of die attach adhesive and molding compound.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

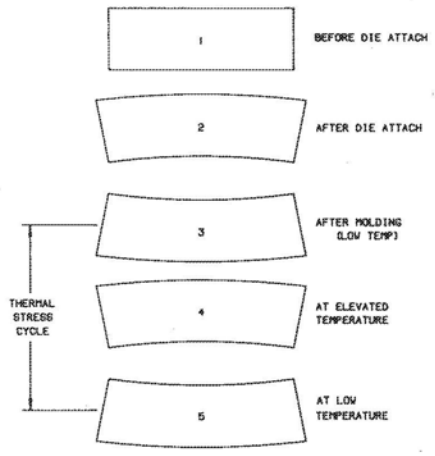


FIGURE 13
Die thermal stress fatigue model.

Die Attach Process: The modeling results show that for both assemblies, with two different leadframe thicknesses, the maximum normal stress on the die surface is tensile and occurs at the center of the chip. Figure 10 shows the tensile stress distribution on the die surface. It can be seen that the stresses gradually decrease towards the chip edges. Though the stress distributions on the die surface are identical in shape for both assemblies, they are different in magnitude. Assembly with the 0.25 mm thick leadframe produced 11.5 kg/mm^2 while assembly with the 0.375 mm thick leadframe produced 10.0 kg/mm^2. The model shows no shear stress on the die surface, which is expected since the surface is in pure bending. However, the chip maximum deflection at the center was 0.92 x 10^{-2} mm and 0.80 x 10^{-2}mm for thinner and thicker leadframes, respectively. This particular finding suggests that using a thicker leadframe in the assembly will produce lower die deflection which, in turn, can lead to a higher resistance to thermal cyclic fatigue during temperature changes that will be elaborated on later in reference to the thermal cyclic model.

Molding Process: Figure 11 shows the stress contours on the die surface at the end of the molding and cure process. Zero stress conditions were assumed at T_g = 155°C. The whole surface is seen to be under compressive stress, with maximum stress concentrated on the die edges parallel to the longitudinal axis and on the corners. The compressive stress distributions are similar for both assemblies but different in magnitude. Assembly with the 0.25 mm thick leadframe yielded 19.5 kg/mm^2 stress on the chip corners, while assembly with the 0.375 mm thick leadframe yielded only 16.5 kg/mm^2. A 15 percent reduction in stress on the chip corners is achieved by using a thicker leadframe in the package. In addition, the die surface shear stress is 12 percent lower for 0.375 mm thick leadframe. The shear stress distribution on the chip surface is the same for both assemblies. As shown in Figure 12, the maximum shear is concentrated on the chip corners and exponentially decreases to zero at the center of the die. [13]

In summary, these comparative results show that the 0.375 mm thick leadframe could be better than the 0.25 mm thick leadframe because (i) the permanent *in-situ* normal and shear stresses produced on the chip surface as a result of either the die attach or the molding processes are lower, (ii) the temperature dependence of the die surface stress is lower, and (iii) the maximum die deflection is also lower. These theoretical findings highlight the potential contribution that the leadframe thickness would have in reducing thermal-fatigue damage and vulnerability of the die to stress caused by temperature changes. To explain this, the following model is postulated.

DIE THERMAL FATIGUE MODEL

At the beginning of the molding process, the die surface is completely under tensile stress, as depicted in Figure 13. At the end of the molding process, at room temperature, the stress reverses to a com-

pressive stress. If the package system is heated again to a higher temperature the compressive stress will reverse to a tensile stress. This reversible process is repeated whenever the package is exposed to temperature excursions, causing the die to deflect in a butterfly-like movement. [14] The reversible deflection is further aggravated by the effects of the superimposed shear force which eventually will lead to a combined vertical and horizontal thermal cyclic strain, particularly on the edges and corners of the die. Ultimately, microcracks will start to grow in the passivation layer. Subsequently, the device metal deformation will initiate.

Based on the analysis of the experimental and analytical results and the model proposed above, we inferred that a lower failure rate should be expected for package systems with thicker leadframes, since the cyclic die deflection and level of stresses will be lower during thermal stress transition. Therefore, less thermal fatigue effects will be induced on the surface of a die that is mounted on this thicker leadframe.

NEW PACKAGE EVOLUTION AND PERFORMANCE EVALUATION

Based upon the modeling predictions and the experimental evidence of thermal and reliability enhancement, the new package system was designed and placed into production. The features of the optimized package are described in Figure 14. Production lot samples of the newly developed package system were thermally characterized and exposed to an extensive reliability qualification study.

THERMAL CHARACTERIZATION

Production samples were thermally characterized under different ambient and cooling conditions. Results are summarized in Table IV. As shown in the table, two modes of cooling at room temperature were used during thermal characterization of the new package: natural convection, and moving air, both with and without a miniature heat sink. In still air at room temperature, the basic power dissipation capability of the new package without a heat sink is 3 W at T_J = 150°C. This represents a 25 and 35 percent improvement over the average and worst performances, respectively (see Table I). The comparison can be seen in Figure 15, which demonstrates the relationship between the thermal resistance and package power dissipation for the new package compared to packages discussed earlier. The boundary line in Figure 15 relates maximum power dissipation of the packages at T_J = 150°C, which is normally specified as the junction temperature safe limit for BiMOS silicon technology. The best absolute thermal improvement with the new package can be achieved in moving air with a heat sink mounted on its web. The maximum steady-state power capability then is 9.1 W.

TABLE IV

NEW PACKAGE SYSTEM THERMAL PERFORMANCE AT T_J = 150°C

No.	Test Conditions	$R_{\theta JA}$(°C/W)	Power Dissipated (W)
1	• Still air (room temp.) • No heat sink	41.6	3.05
2	• Still air (room temp.) • Heat sink (staver type)	24.8	5.1
3	• Moving air (200 LFM) • Room temperature • No heat sink	25.8	4.9
4	• Moving air (200 LFM) • Room temperature • Heat sink	13.9	9.10

QUALIFICATION TEST PROGRAM

The following were the qualification tests conducted:

1 - High-temperature reverse bias life test—150°C ambient at 50 V applied.
2 - Biased 85°C/85 percent RH test at 50 V applied.
3 - Pressure cooker—121°C, 100 percent RH.
4 - Extended temperature cycle, (-65°C + 150°C).
5 - Thermal resistance, $R_{\theta JA}$ after each interval of 500 temperature cycles.

No failures have been reported to date in any of the tests. Results are summarized in Table V.

SUMMARY AND CONCLUSIONS

A high-performance, unconventional 16-lead Plastic Dual-In-Line Package has been developed. The new package power dissipation capability is 25 percent higher than the average measured for available packages and 35 percent higher than the worst package. The long-term reliability performance of the new package exceeds present industry standard reliability requirements. Reliability data also show

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

TABLE V

RELIABILITY QUALIFICATION RESULTS FOR NEW 16-LEAD DIP

No.	Test	No. of Hours or Cycles Completed	Sample Size	Number of Failures
1	150°C HTRB	6000 h	100	0
2	85°C/85 percent RH/Bias	6000 h	50	0
3	Temp. cycle - 65°C + 150°C "Electrical"	10 000 C	50	0
4	Temperature cycling, "Thermal resistance"	9000 C	12	0
5	Temperature cycling (ground wire fatigue life)	9000 C	50	0

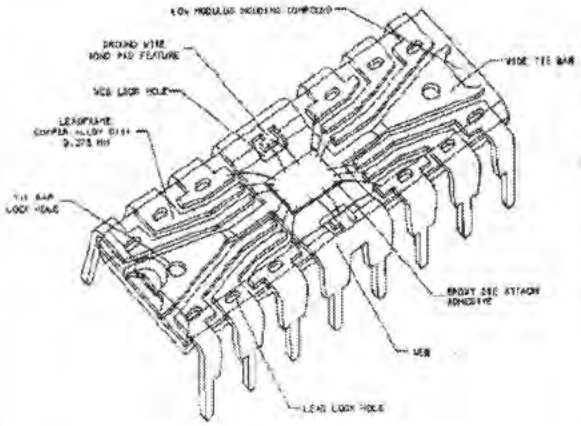


FIGURE 14

New web 16-lead PDIP.

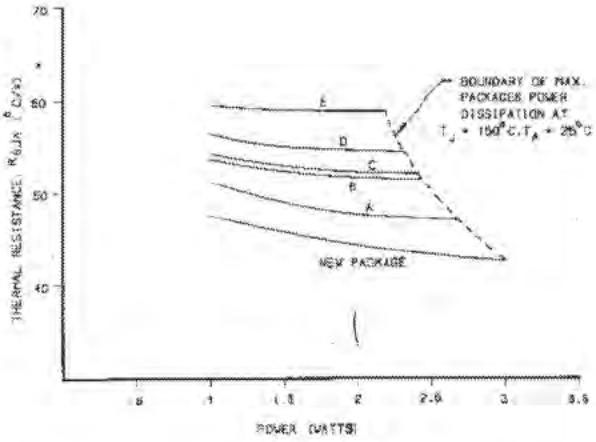


FIGURE 15

Thermal resistance versus power dissipation capability for various packages.

that the chip surface metal deformation resistance to temperature cycling is improved by a factor of 4, and the ground wire propensity for thermal cyclic fatigue damage has been reduced by a factor of 7.

The superiority of the package is due to a combination of an optimum leadframe design and proper choice of materials, such as a low-modulus molding compound. The development strategy was based on a package optimization approach, in which a comparative analysis indicated that existing packages are not fully optimized. Extensive thermal and thermostructural studies have been performed. The finite element results have provided an insight into both the thermal and structural performance of the package.

REFERENCES

[1] C. Mitchell and H. Berg, "Thermal Studies of Plastic Dual-In-Line Package," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-2, pp. 500-511, December 1979.

[2] J. A. Andrews et al., "Thermal Characteristics of 16 and 40 Pin Plastic DIP Packages," IEEE Trans actions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-4, pp. 455-461, December 1981.

[3] W. H. Schroen et al., "Reliability Tests and Stress in Plastic Integrated Circuits," in Proceedings 19th Annual Reliability Physics Symposium, pp. 81-87, 1981.

[4] M. Aghazadeh and B. Natarajan, "Parametric Study of Heatspreader Thermal Performance in 48 Lead Plastic DIPs and 68 Lead Plastic Leaded Chip Carriers," in Proceedings 36th Electronic Components Conference, pp.143-149, 1986.

[5] K. Kuwata, K. Iko, and T. Tabata, "Low Stress Resin Encapsulants for Semiconductor Devices," in Proceedings 35th Electronic Components Conference, pp.18-23, 1985.

[6] S. Ito et al., "Special Properties of Molding Compounds for Large Surface-Mounting Devices", in Proceedings 38th Electronics Components Conference, pp. 486-492, 1988.

[7] J. Dais and F. Howland, "Fatigue Failure of Encapsulated Gold-Beam lead and TAB devices," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-1, pp.158-166, June 1978.

[8] J. H. Faupel and F. E. Fisher, Engineering Design, New York, N.Y.: Wiley-Interscience Publication, CH.15, pp. 973-977, 1981.

[9] K. R. Kinsman, "The Mechanics of Molded Plastic Packages," Journal of Metals, pp. 23-29, June 1988.

[10] M. Isagawa et al., "Deformation of Al Metallization in Plastic Encapsulated Semiconductor Devices Caused by Thermal Shock," in Proceedings 18th Annual Reliability Physics Symposium, pp. 171-177, 1980.

[11] R. E. Thomas, "Stress-Induced Deformation of Aluminum Metallization in Plastic Molded Semiconductor Devices," in Proceedings 35th Electronic Components Conference, pp. 37-45, 1985.

[12] R. J. Usell and S. A. Smiley, "Experimental and Mathematical Determination of Mechanical Strains Within Plastic IC Packages and Their Effect on Devices During Environmental Tests", in Proceed ings 19th Annual Reliability Physics Symposium, pp. 65-73, 1981.

[13] S. Okikawa et al., "Stress Analysis of Passivation Film Cracks for Plastic Molded LSI Caused by Thermal Stress," in Proceedings International Symposium for Testing and Failure Analysis, pp. 275-280, 1983.

[14] S. Sasaki et al., "The Development of Mini Plastic IC Packaging for DIP Soldering," in Proceedings 34th Electronic Components Conference, pp. 383-387, 1984.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

EXHIBIT 13

STANDARD ST.9

RECOMMENDATION CONCERNING BIBLIOGRAPHIC DATA ON
AND RELATING TO PATENTS AND SPCS

Editorial Note prepared by the International Bureau

Users of patent documents and Patent Gazettes often encounter difficulties in identifying the bibliographic data on or concerning patent documents. The aim of this Recommendation is to overcome these difficulties. The Recommendation covers a list of approximately 60 distinct bibliographic data widely used on the first page of patent documents or in Patent Gazettes. They are identified through code numbers, the so-called "INID Codes" or "INID Numbers". ("INID" is an acronym for "Internationally agreed Numbers for the Identification of (bibliographic) Data".)

The bibliographic data covered in the Recommendation range from data for the document identification, filing data, priority data, publication data, data concerning technical information to data related to International Patent Conventions.

STANDARD ST.9

RECOMMENDATION CONCERNING BIBLIOGRAPHIC DATA ON
AND RELATING TO PATENTS AND SPCS

(Identification and Minimum requirements)

Revision adopted by the Committee on WIPO Standards (CWS)
at its third session on April 19, 2013

INTRODUCTION

1. This Recommendation is aimed at improving the access to information relating to patents and SPCs in general and to the bibliographic content of Patent Gazettes and patent documents in particular.

2. This Recommendation provides for codes whereby the various bibliographic data appearing on the first page of a patent document and/or in an entry in a Patent Gazette can be identified without knowledge of the language used and the industrial property laws, conventions or treaties applied.

3. This Recommendation further indicates the bibliographic data which as a *minimum* should be printed on the first page of a patent document and be published as part of an entry in a Patent Gazette.

DEFINITIONS

4. For the purposes of this Recommendation, the expression:

(a) "patents" includes such industrial property rights as patents for inventions, plant patents, design patents, inventors' certificates, utility certificates, utility models, patents of addition, inventors' certificates of addition and utility certificates of addition;

(b) "SPCs" stands for supplementary protection certificates. The SPC takes effect at the end of the term of a patent which protects the product as such, a process to obtain the product or an application of the product. For a detailed definition of an SPC, please refer to the Glossary of Terms Concerning Industrial Property Information and Documentation, which is published in Part 8, of the WIPO *Handbook on Industrial Property Information and Documentation*;

(c) "patent documents" means documents containing bibliographic data and other information with respect to such industrial property rights as patents for inventions, plant patents, design patents, inventors' certificates, utility certificates, utility models, patents of addition, inventors' certificates of addition, utility certificates of addition, and published applications therefor;

(d) "Patent Gazette" means a journal containing announcements with respect to patents and SPCs made in accordance with requirements under national industrial property laws or regional or international industrial property conventions or treaties;

(e) "entry in a Patent Gazette" means a comprehensive announcement including bibliographic data made in a Patent Gazette regarding patents and SPCs or applications therefor;

(f) "making available to the public" means:

(i) publishing multiple copies of a patent document produced on, or by, any medium (e.g., paper, film, magnetic tape or disc, optical disc, online database, computer network, etc.) or

(ii) laying open for public inspection and supplying a copy on request;

(g) "examined" and "unexamined" refer to an examination made as to substance, as distinct from the preparation of a documentary search report or an examination made as to form which latter examination is ordinarily made by an industrial property office immediately upon receipt of an application;

(h) "INID" is an acronym for "Internationally agreed Numbers for the Identification of (bibliographic) Data".

5. References to the following Standards are of relevance to this Recommendation:

WIPO Standard ST.2	Standard Manner for Designating Calendar Dates by Using the Gregorian Calendar;
WIPO Standard ST.3	Recommended Standard on Two-Letter Codes for the Representation of States, Other Entities and Intergovernmental Organizations;
WIPO Standard ST.10/B	Layout of Bibliographic Data Components;
WIPO Standard ST.10/C	Presentation of Bibliographic Data Components;
WIPO Standard ST.14	Recommendation for the Inclusion of References Cited in Patent Documents;
WIPO Standard ST.16	Recommended Standard Code for the Identification of Different Kinds of Patent Documents;
WIPO Standard ST.18	Recommendation Concerning Patent Gazettes and Other Patent Announcement Journals;
WIPO Standard ST.34	Recommendation Concerning the Recording of Application Numbers in Electronic Form for the Exchange of Bibliographic Data;
WIPO Standard ST.50	Guidelines for Issuing Corrections, Alterations and Supplements relating to Patent Information

International Standard ISO 639:1988 “Code for the Representation of Names of Languages”.

IDENTIFICATION OF BIBLIOGRAPHIC DATA AND MINIMUM REQUIREMENTS

6. The list of definitions of bibliographic data with their corresponding INID codes is given in Appendix 1 to this Recommendation and entitled “INID codes and minimum requirements for the identification of bibliographic data elements”. To assist industrial property offices and users of industrial property documentation, Appendix 2 to this Recommendation contains those INID codes, with their definitions and/or notes, which were used at a certain period of time but have either ceased to be available for use or have been amended.

7. The INID codes which are preceded by a single asterisk (*) relate to those data elements which are considered to be the minimum elements which should appear on the first page of a patent document and in an entry in a Patent Gazette. In this Standard, no minimum data elements are defined relating to SPCs.

8. The INID codes which are preceded by a double asterisk (**) relate to those data elements which are considered to be minimum elements in circumstances specified in the accompanying notes.

APPLICATION OF CODES

9. The INID codes should be associated with the corresponding bibliographic data in so far as these data normally appear on the first page of a patent document or in an entry in a Patent Gazette.

10. Provided the presentation of bibliographic data in entries in a Patent Gazette is uniform, INID codes may be applied to the bibliographic data in a representative specimen entry in each gazette issued, instead of being included in each entry.

11. The INID codes should be printed in Arabic numerals, preferably within small circles or if this is not possible, in parentheses, immediately *before* the corresponding bibliographic data element.

12. If bibliographic data to which INID codes are assigned in accordance with this Recommendation do not appear on the first page of a patent document or in an entry in a Patent Gazette—because they are not applicable (e.g., when no priority is claimed) or for some other reason—it is not necessary to call attention to the non-existence of such elements (e.g., by leaving a space or by providing the relevant INID code followed by a dash).

13. Two or more INID codes may be assigned to a single bibliographic data when necessary.

14. The list of bibliographic data has been organized into categories to facilitate grouping of related data. Each category has several subdivisions to each of which an INID code has been assigned. Category codes, ending in "0", can themselves be used in one, or both, of the following situations:

(a) where several individual bibliographic data items of the same category are present and it is desired to present those individual data items together without using individual INID codes;

(b) where INID codes are not provided for specific bibliographic data items.

Industrial property offices should clearly define the use by them of category codes in each of the above situations.

15. The presentation of calendar dates identified by any of the INID codes concerned should be in the sequence and format as recommended in WIPO Standard ST.2.

16. In order that the users of patent documents and Patent Gazettes may be enabled to make maximum use of the INID codes, it is recommended that a list of the codes be published in Patent Gazettes at regular intervals (see WIPO Standard ST.18).

IMPLEMENTATION

17. Industrial property offices can start using this Recommendation at any time. It is recommended that when implementing the INID codes an announcement in the sense of paragraph 16 be made and the International Bureau of WIPO be informed, e.g., by forwarding a sample of the Patent Gazette.

[Appendix 1 follows]

APPENDIX 1

INID CODES AND MINIMUM REQUIREMENTS FOR THE IDENTIFICATION
OF BIBLIOGRAPHIC DATA ELEMENTS

(10) Identification of the patent, SPC or patent document

* (11) Number of the patent, SPC or patent document

* (12) Plain language designation of the kind of document

* (13) Kind-of-document code according to WIPO Standard ST.16

(15) Patent correction information

** (19) WIPO Standard ST.3 code, or other identification, of the office or organization publishing the document

Notes: (i) For an SPC, data regarding the basic patent should be coded by using code (68).

(ii) ** Minimum data element for patent documents only.

(iii) With the proviso that when data coded (11) and (13), or (19), (11) and (13), are used together and on a single line, category (10) can be used, if so desired.

(iv) Data to be given under code (15) should be presented in accordance with the provisions set out in WIPO Standard ST.50.

(20) Data concerning the application for a patent or SPC

* (21) Number(s) assigned to the application(s), e.g., “Numéro d’enregistrement national”, “Aktenzeichen”

* (22) Date(s) of filing the application(s)

* (23) Other date(s), including date of filing complete specification following provisional specification and date of exhibition

(24) Date from which industrial property rights may have effect

(25) Language in which the published application was originally filed

(26) Language in which the application is published

(27) Reference to a previously filed application for the purpose of obtaining a filing date under the Patent Law Treaty (PLT), Article 5(7)

Notes: (i) The document "Terms of Protection", which provided information related to code (24), has been moved to the Archives.

(ii) The languages under codes (25) and (26) should be indicated by using the two-letter language symbols according to International Standard ISO 639:1988.

(iii) With regard to code (27), the reference shall be made by indicating the WIPO Standard ST.3 code of the office with which the previous application was filed, the application number of the application, and, if required, the filing date.

* For the meaning of the asterisk, see paragraph 7 or 8 of this Recommendation.

Appendix 1, page 2

(30) Data relating to priority under the Paris Convention or the Agreement on Trade-Related Aspects of Intellectual Property Rights (TRIPS Agreement)

* (31) Number(s) assigned to priority application(s)

* (32) Date(s) of filing of priority application(s)

* (33) WIPO Standard ST.3 code identifying the national industrial property office allotting the priority application number or the organization allotting the regional priority application number; for international applications filed under the PCT, the code "WO" is to be used

(34) For priority filings under regional or international arrangements, the WIPO Standard ST.3 code identifying at least one country party to the Paris Convention or member of the World Trade Organization for which the regional or international application was made

Notes: (i) With the proviso that when data coded (31), (32) and (33) are presented together, category (30) can be used, if so desired. If an ST.3 code identifying a country for which a regional or international application was made is published, it should be identified as such using code (34) and should be presented separately from elements coded (31), (32) and (33) or (30).

(ii) The presentation of priority application numbers should be as recommended in WIPO Standards ST.10/C and in ST.34.

(40) Date(s) of making available to the public

** (41) Date of making available to the public by viewing, or copying on request, an unexamined patent document, on which no grant has taken place on or before the said date

** (42) Date of making available to the public by viewing, or copying on request, an examined patent document, on which no grant has taken place on or before the said date

** (43) Date of making available to the public by printing or similar process of an unexamined patent document, on which no grant has taken place on or before the said date

** (44) Date of making available to the public by printing or similar process of an examined patent document, on which no grant or only a provisional grant has taken place on or before the said date

** (45) Date of making available to the public by printing or similar process of a patent document on which grant has taken place on or before the said date

(46) Date of making available to the public the claim(s) only of a patent document

** (47) Date of making available to the public by viewing, or copying on request, a patent document on which grant has taken place on or before the said date

* (48) Date of issuance of a corrected patent document

Note: ** Minimum data element for patent documents only, the minimum data requirement being met by indicating the date of making available to the public the patent document concerned.

(50) Technical information

* (51) International Patent Classification or, in the case of a design patent, as referred to in subparagraph 4(c) of this Recommendation, International Classification for Industrial Designs

(52) Domestic or national classification

* (54) Title of the invention

(56) List of prior art documents, if separate from descriptive text

(57) Abstract or claim

Appendix 1, page 3

(58) Field of search

Notes: (i) The presentation of the classification symbols of the International Classification for Industrial Designs should be made in accordance with paragraph 4 of WIPO Standard ST.10/C.

(ii) With regard to code (56) attention is drawn to WIPO Standard ST.14 in connection with the citation of references on the first page of patent documents and in search reports attached to patent documents.

(60) References to other legally or procedurally related domestic or previously domestic patent documents including unpublished applications therefor

* (61) Number and, if possible, filing date of the earlier application, or number of the earlier publication, or number of earlier granted patent, inventor's certificate, utility model or the like to which the present patent document is an addition

* (62) Number and, if possible, filing date of the earlier application from which the present patent document has been divided up

* (63) Number and filing date of the earlier application of which the present patent document is a continuation

* (64) Number of the earlier publication which is "reissued"

(65) Number of a previously published patent document concerning the same application

(66) Number and filing date of the earlier application of which the present patent document is a substitute, i.e., a later application filed after the abandonment of an earlier application for the same invention

(67) Number and filing date of a patent application, or number of a granted patent, on which the present utility model application or registration (or a similar industrial property right, such as a utility certificate or utility innovation) is based

(68) For an SPC, number of the basic patent and/or, where appropriate, the publication number of the patent document

Notes: (i) Priority data should be coded in category (30).

(ii) Code (65) is intended primarily for use by countries in which the national laws require that re-publication occur at various procedural stages under different publication numbers and these numbers differ from the basic application numbers.

(iii) Category code (60) should be used by countries which were previously part of another entity for identifying bibliographic data elements relating to applications or grants of patents which data had initially been announced by the industrial property office of that entity.

(70) Identification of parties concerned with the patent or SPC

** (71) Name(s) of applicant(s)

(72) Name(s) of inventor(s) if known to be such

** (73) Name(s) of grantee(s), holder(s), assignee(s) or owner(s)

(74) Name(s) of attorney(s) or agent(s)

** (75) Name(s) of inventor(s) who is (are) also applicant(s)

** (76) Name(s) of inventor(s) who is (are) also applicant(s) and grantee(s)

Notes: (i) ** For patent documents for which grant has taken place on or before the date of making available to the public, and gazette entries relating thereto, the minimum data requirement is met by indicating the grantee, and for other documents by indication of the applicant.

(ii) Codes (75) and (76) are intended primarily for use by countries in which the national laws require that the inventor and applicant be normally the same. In other cases codes (71) or (72) or (71), (72) and (73) should generally be used.

Appendix 1, page 4

(80) (90) Identification of data related to International Conventions other than the Paris Convention, and to legislation with respect to SPCs

(81) Designated State(s) according to the PCT

(83) Information concerning the deposit of microorganisms, e.g., under the Budapest Treaty

(84) Designated Contracting States under regional patent conventions

(85) Date of commencement of the national phase pursuant to PCT Article 23(1) or 40(1)

(86) Filing data of the PCT international application, i.e., international filing date, international application number, and, optionally, the language in which the published international application was originally filed; or, in the case of design patents, registration data of the Hague Agreement international application, i.e., international registration date and international registration number

(87) Publication data of the PCT international application, i.e., international publication date, international publication number, and, optionally, the language in which the international application is published

(88) Date of deferred publication of the search report

(91) Date on which an international application filed under the PCT no longer has an effect in one or several designated or elected States due to failure to enter the national or regional phase or the date on which it has been determined that it had failed to enter the national or regional phase

(92) For an SPC, number and date of the first national authorization to place the product on the market as a medicinal product or plant protection product

(93) For an SPC, number, date and, where applicable, country of origin, of the first authorization to place the product on the market as a medicinal product or plant protection product within a regional economic community

(94) Calculated date of expiry of the SPC or the duration of the SPC

(95) The product protected by the basic patent and in respect of which the SPC or the extension of the SPC has been applied for or granted

(96) Filing data of the regional application, i.e., application filing date, application number, and, optionally, the language in which the published application was originally filed

(97) Publication data of the regional application (or of the regional patent, if already granted), i.e., publication date, publication number, and, optionally, the language in which the application (or, where applicable, the patent) is published

(98) For an SPC, the date concerning the application for an extension of the duration, the revocation of an extension of the duration and the recalculation of the duration

Notes: (i) With regard to patents for invention, the codes (86), (87), (96) and (97) are intended to be used:

– on national documents when identifying one or more of the relevant filing data or publication data of the PCT international application or of the regional application (or of the regional patent, if already granted), or

– on regional documents when identifying one or more of the relevant filing data or publication data of the PCT international application or of another regional application (or the regional patent, if already granted).

(ii) All data in codes (86), (87), (96) or (97) should be presented together and preferably on a single line. The application number or publication number should comprise the three basic elements as shown in the examples in paragraph 17 of WIPO Standard ST.10/B.

(iii) When data to be referenced by codes (86), (87), (96) or (97) refer to two or more PCT international applications and/or regional applications (or regional patents, if already granted), each set of relevant filing or publication data of each such application (or granted patent) should be displayed so as to be clearly distinguishable from other sets of relevant data, e.g., by presenting each set on a single line or by presenting the data of each set grouped together on adjacent lines in a column with a blank line between each set.

Appendix 1, page 5

(iv) The languages under codes (86), (87), (96) and (97) should be indicated by using the two-letter language symbols according to International Standard ISO 639:1988.

(v) The country of origin in code (93), if mentioned, should be indicated by using the two-letter code according to WIPO Standard ST.3.

(vi) The document "Terms of Protection", which provided information related to code (24), has been moved to the Archives.

[Appendix 2 follows]

APPENDIX 2

DELETIONS AND AMENDMENTS TO THE CODE LIST GIVEN IN APPENDIX 1

INID Code	Previous definition(s) of code	Pertinent previous note(s)	Date of deletion or amendment	Kind of change
(15)	Patent Correction Information	–	May 28, 1998, by PCIPI/EXEC/XXII	Footnote added
(30)	Data relating to priority under the Paris Convention		February 21, 2008, by SCIT/SDWG/9	Code definition amended
(34)	For priority filings under regional or international arrangements, the WIPO Standard ST.3 code identifying at least one country party to the Paris Convention for which the regional or international application was made		February 21, 2008, by SCIT/SDWG/9	Code definition amended
(51)	International Patent Classification	–	November 29, 1996, by PCIPI/EXEC/XIX	Code definition amended
(53)	Universal Decimal Classification	–	November 21, 1997, by PCIPI/EXEC/XXI	Code deleted
(55)	Keywords	–	November 21, 1997, by PCIPI/EXEC/XXI	Code deleted
(73)	Name(s) of grantee(s) or of the holder(s)	–	November 29, 1996, by PCIPI/EXEC/XIX	Code definition amended
(85)	Date of fulfillment of the requirements of Articles 22 and/or 39 of the PCT for introducing the national procedure according to the PCT	–	May 30, 1997, by PCIPI/EXEC/XX	Code definition amended

Appendix 2, page 2

INID Code	Previous definition(s) of code	Pertinent previous note(s)	Date of deletion or amendment	Kind of change
(86)	Filing data of the regional or PCT application, i.e., application filing date, application number, and, optionally, the language in which the published application was originally filed	(i) The codes (86) and (87) are intended to be used: – on national documents when identifying one or more of the relevant filing data or publication data of the regional application (or of the regional patent, if already granted) or of the PCT application, or – on regional documents when identifying one or more of the relevant filing data or publication data of another regional application (or a regional patent, if already granted) or of a PCT application. (ii) All data in code (86), or in code (87), should be presented together and preferably on a single line. The publication number should comprise the three basic elements as shown in the examples in paragraph 17 of WIPO Standard ST.10/B. (iii) When data to be referenced by codes (86) or (87) refer to two or more regional applications (or regional patents, if already granted) and/or PCT applications, each set of relevant filing or publication data of each such application (or granted patent) should be displayed so as to be clearly distinguishable from other sets of relevant data, e.g., by presenting each set on a single line or by presenting the data of each set grouped together on adjacent lines in a column with a blank line between each set.	November 21, 1997, by PCIPI/EXEC/XXI	Code definition and notes amended
(86)	Filing data of the PCT international application, i.e., international filing date, international application number, and, optionally, the language in which the published international application was originally filed	(i) The codes (86), (87), (96) and (97) are intended to be used: – on national documents when identifying one or more of the relevant filing data or publication data of the PCT international application or of the regional application (or of the regional patent, if already granted), or – on regional documents when identifying one or more of the relevant filing data or publication data of the PCT international application or of another regional application (or the regional patent, if already granted).	January 30, 2004, by SCIT/SDWG/4	Code definition and note amended

Appendix 2, page 3

INID Code	Previous definition(s) of code	Pertinent previous note(s)	Date of deletion or amendment	Kind of change
(87)	Publication data of the regional or PCT application, i.e., publication date, publication number, and, optionally, the language in which the application is published	(i) The codes (86) and (87) are intended to be used: – on national documents when identifying one or more of the relevant filing data or publication data of a regional or PCT application, or – on regional documents when identifying one or more of the relevant filing data or publication data of another regional or PCT application. (ii) All data in code (86), or in code (87), should be presented together and preferably on a single line. (iii) When data to be referenced by INID codes (86) or (87) refer to two or more regional and/or PCT applications, each set of relevant filing or publication data of each such application should be displayed so as to be clearly distinguishable from other sets of relevant data, e.g., by presenting each set on a single line or by presenting the data of each set grouped together on adjacent lines in a column with a blank line between each set.	May 30, 1997, by PCIPI/EXEC/XX	Code definition and notes amended
(87)	Publication data of the regional application (or of the regional patent, if already granted) or of the PCT application, i.e., publication date, publication number, and, optionally, the language in which the application is published	(i) The codes (86) and (87) are intended to be used: – on national documents when identifying one or more of the relevant filing data or publication data of the regional application (or of the regional patent, if already granted) or of the PCT application, or – on regional documents when identifying one or more of the relevant filing data or publication data of another regional application (or a regional patent, if already granted) or of a PCT application. (ii) All data in code (86), or in code (87), should be presented together and preferably on a single line. The publication number should comprise the three basic elements as shown in the examples in paragraph 17 of WIPO Standard ST.10/B. (iii) When data to be referenced by codes (86) or (87) refer to two or more regional applications (or regional patents, if already granted) and/or PCT applications, each set of relevant filing or publication data of each such application (or granted patent) should be displayed so as to be clearly distinguishable from other sets of relevant data, e.g., by presenting each set on a single line or by presenting the data of each set grouped together on adjacent lines in a column with a blank line between each set.	November 21, 1997, by PCIPI/EXEC/XXI	Code definition and notes amended

Appendix 2, page 4

INID Code	Previous definition(s) of code	Pertinent previous note(s)	Date of deletion or amendment	Kind of change
(89)	Document number, date of filing, and country of origin of the original document according to the CMEA Agreement on Mutual Recognition of Inventors' Certificates and other Titles of Protection for Inventions	(iv) With regard to code (89), it should be noted that the CMEA ceased to exist in 1991.	November 21, 1997, by PCIPI/EXEC/XXI	Code and note deleted
(92)	For an SPC, number and date of the first national authorization to place the product on the market as a medicinal product	–	April 19, 2013, by CWS/3	Code definition amended
(93)	For an SPC, number, date and, where applicable, country of origin, of the first authorization to place the product on the market as a medicinal product within a regional economic community	–	April 19, 2013, by CWS/3	Code definition amended
(95)	Name of the product protected by the basic patent and in respect of which the SPC has been applied for or granted	–	April 19, 2013, by CWS/3	Code definition amended

[End of Standard]

EXHIBIT 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC d/b/a
ON SEMICONDUCTOR
Petitioner

v.

POWER INTEGRATIONS, INC.
Patent Owner

Case No. Unassigned
Patent 6,538,908

PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1, 3, 4, 5, 9, 10, 19, 20, 22, 23, 24, 30, 31, 32, 33, AND 34 OF U.S. PATENT NO. 6,538,908

The Current Mirror circuit performs two functions in response to the current signal "I": (i) it generates and sends a current-limit adjustment signal to the "Current Limit Comparator," and (ii) it generates an oscillator frequency adjustment signal that is sent to the "Oscillator." Ex. 1003, ¶ 37; Ex. 1005, 7 (Fig. 17), 8.

2. Shinji

Japanese Unexamined Patent Application Publication No. H10-108457 ("Shinji") was published by the Japanese Patent Office and publicly available on April 24, 1998 (*see* Ex. 1022, 3), which is over one year prior to the claimed September 24, 1999 priority date of the '908 Patent (*see* Ex. 1001). Shinji thus qualifies as § 102(b) prior art. Shinji was not considered during the original prosecution of the '908 Patent, during either reexamination of the '908 Patent, during the ITC Matter, or during the N.D. California or the System General Litigation. *See* Ex. 1001, [56]; Ex. 1002, 1–3; Ex. 1018, 128; Ex. 1019, 2.

Like the '908 Patent, Shinji discloses a power supply controller (i.e., switching regulator) designed to operate from a rectified AC voltage source. Ex. 1022, ¶ 21, 23 (Fig. 23); Ex. 1003, ¶ 39. Also like the '908 Patent, Shinji recognizes the advantages of a control IC with a low pin count that can be configured with a low number of external components. Ex. 1022, ¶ 14 ("The number of pins is small, and since it is possible to reduce the number of external

VII. CONCLUSION

Petitioner respectfully requests that *inter partes* review of the '908 Patent be instituted and that claims 1, 3, 4, 5, 9, 10, 19, 20, 22, 23, 24, 30, 31, 32, 33, and 34 be cancelled as unpatentable under 35 U.S.C. § 318(b).

Respectfully submitted,
BAKER BOTTS L.L.P.

August 11, 2016
Date

/Roger Fulghum/
Roger Fulghum (Reg. No. 39,678)
One Shell Plaza
910 Louisiana Street
Houston, Texas 77002-4995

Lead Counsel for Petitioner

EXHIBIT 15

(19) Japan Patent Office (JP) (12) JAPANESE UNEXAMINED PATENT APPLICATION PUBLICATION (A) (11) Patent Application Disclosure No. **H10-108457**

(43) Publication Date April 24, 1998 (Heisei 10)

(51) Int. Cl.[6]		Ident. Code	FI		
H 02 M	3/28		H 02 M	3/28	C
					B
G 05 F	1/56	310	G 02 F	1/56	310 C
H 02 H	7/12		H 02 H	7/12	G

Examination Request: Not Yet Total No. of Claims: 2 OL (Total 14 pages)

(21) Application No. JPA H8-258950

(22) Date of Filing September 30, 1996 (Heisei 8)

(71) Applicant 000002185
Sony Co., Ltd.
6-7-35 Kita-Shinagawa, Shinagawa-ku, Tokyo

(72) Inventor Kaneko Shinji
c/o Sony Co., Ltd.
6-7-35 Kita-Shinagawa, Shinagawa-ku, Tokyo

(54) Title of Invention: SWITCHING POWER SUPPLY CONTROL CIRCUIT

(57) ABSTRACT

Problem: To implement a switching power supply control circuit that shortens the time from overvoltage detection to shutdown in an overvoltage protector circuit.

Resolution Means: A switching power supply control circuit providing a soft start terminal having a function for stopping an overcurrent at the start of an operation and a latch mode cutoff terminal having a function for stopping the switching independently of the other terminal and holds the output to 0, and equipping a common terminal CS connected to a power supply Vcc by a series circuit composed of a current limiting resistor element R1 and a control active element PC1, wherein a capacitance element C0 is provided in parallel to the current limiting resistor element R1.

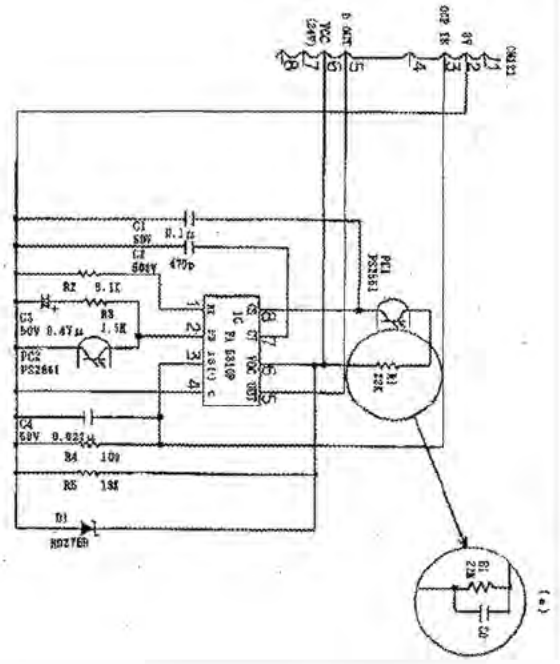


EXHIBIT 16

REDACTED IN ITS ENTIRETY

EXHIBIT 17

REDACTED IN ITS ENTIRETY

EXHIBIT 18

Definition of *extend*

transitive verb

1 : to spread or stretch forth : unbend extended both her arms
2a : to stretch out to fullest length
b : to cause (an animal, such as a horse) to move at full stride
c : to exert (oneself) to full capacity could work long and hard without seeming to extend himself
d(1) : to increase the bulk of (as by adding a cheaper substance or a modifier)
(2) : adulterate

3 [Middle English, from Medieval Latin *extendere* (from Latin) or Anglo-French *estendre*, from Old French]

a British : to take possession of (something, such as land) by a writ of extent
b obsolete : to take by force
4a : to make the offer of : proffer extending aid to the needy extending their greetings
b : to make available extending credit to customers
5a : to cause to reach (as in distance or scope) national authority was extended over new territories
b : to cause to be longer : prolong extend the side of a triangle extended their visit another day also : to prolong the time of payment of
c : advance, further extending her potential through job training
6a : to cause to be of greater area or volume : enlarge extended the patio to the back of the house
b : to increase the scope, meaning, or application of : broaden beauty, I suppose, opens the heart, extends the consciousness— Algernon Blackwood
c archaic : exaggerate

intransitive verb

1 : to stretch out in distance, space, or time : reach their jurisdiction extended over the whole area
2 : to reach in scope or application his concern extends beyond mere business to real service to his customers

Other Words from *extend* Synonyms & Antonyms Choose the Right Synonym More Example Sentences Learn More about *extend*

Keep scrolling for more

Other Words from *extend*

extendability \ ik-ˌsten-də-ˈbi-lə-tē \ noun
extendable or less commonly extendible \ ik-ˈsten-də-bəl \ adjective

Synonyms & Antonyms for *extend*

Synonyms

drag (out), draw out, elongate, lengthen, outstretch, prolong, protract, stretch

Antonyms

abbreviate, abridge, curtail, cut, cut back, shorten

Visit the Thesaurus for More

EXHIBIT 19

REDACTED IN ITS ENTIRETY

EXHIBIT 20

REDACTED IN ITS ENTIRETY

EXHIBIT 21

REDACTED IN ITS ENTIRETY

EXHIBIT 22

REDACTED IN ITS ENTIRETY

EXHIBIT 23

REDACTED IN ITS ENTIRETY

EXHIBIT 24

REDACTED IN ITS ENTIRETY

EXHIBIT 25

REDACTED IN ITS ENTIRETY

EXHIBIT 26

REDACTED IN ITS ENTIRETY

EXHIBIT 27

FIG.4

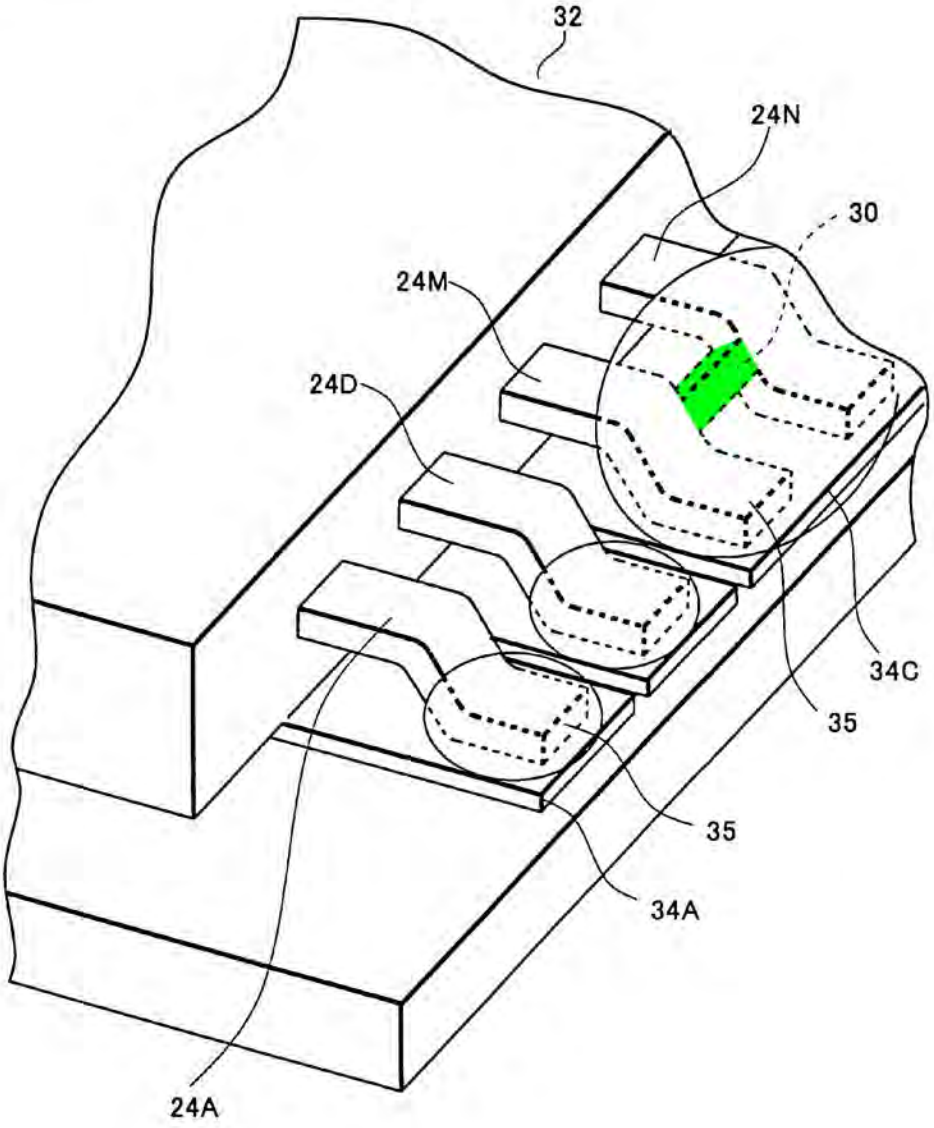


EXHIBIT 28

(19) Japan Patent Office (JP)

(12) **(UNEXAMINED) PATENT APPLICATION PUBLICATION (A)**

(11) Patent Application Publication Number: S61-80842

(43) Publication Date: April 24, 1986

(51) Int. Cl.[4]	Identification Symbol	Office File No.
H01L 23/34		6616-5F

Request for Examination: Not yet requested Number of Inventions: 1
(Total of 3 pages)

(54) Title of the Invention: Semiconductor Device
(21) Application No.: S59-201747
(22) Application Date: September 28, 1984

(72) Inventor: Shigeo Otaka
c/o Takasaki Works, Hitachi, Ltd.
111 Nishiyokotemachi, Takasaki-shi

(72) Inventor: Usuke Enomoto
c/o Takasaki Works, Hitachi, Ltd.
111 Nishiyokotemachi, Takasaki-shi

(72) Inventor: Tetsuro Iijima
c/o Takasaki Works, Hitachi, Ltd.
111 Nishiyokotemachi, Takasaki-shi

(71) Applicant: Hitachi, Ltd.
4-6 Kandasurugadai, Chiyoda-ku, Tokyo

(74) Agent: Patent Attorney Akio Takahashi and one other

Specification

Title of the Invention: Semiconductor Device

Claims

1. A semiconductor device wherein a heat dissipation plate equal to or larger than the distance between at least two external connection pins is formed at an external connection pin.

Detailed Description of the Invention

(Technical Field)

[1] The present invention relates to a semiconductor device and in particular to a technology that is well suited for use in a transistor or a semiconductor integrated circuit for high output power use where a superior heat dissipation effect is required.

(Background Art)

[2] With transistors used for high output power, it is no exaggeration to state that the output power is determined by whether or not the heat dissipation effect is good. Thus, various proposals have been made in regards to the heat dissipation plates of semiconductor devices. Bearing in mind heat dissipation in output transistors where the output power may exceed, for example, 1W, the present inventors conducted various technical studies and arrived at the present invention.

[3] It should be noted that Unexamined Patent Application Publication No. S57-177548 discloses a proposal regarding a heat dissipation plate.

(Object of the Invention)

[4] It is the object of the present invention to provide a semiconductor device capable of performing superior heat dissipation by using external connection pins.

[5] The afore-described and other objects and novel features of the present invention would become clear from the description in the specification and the attached drawings.

(Summary of the Invention)

[6] The invention that is disclosed in this application can be simply summarized as follows.

[7] In the context of a transistor, the object of the present invention is achieved by forming, at an external connection pin that is connected to the collector, a large heat dissipation plate equal to or larger than the distance between two external connection pins.

Embodiment 1

[8] A first embodiment of a semiconductor device applying the present invention is described next with reference to FIG. 1 through FIG. 3. The present embodiment is an example of use in a high output power transistor.

[9] First, to describe the structure of the frame shown in FIG. 1, 1 is a tab on whose top surface is disposed a semiconductor chip 2 outlined by the dotted lines. The semiconductor chip 2 is large as shown by the dotted lines when it is used to achieve a high output power, but the size is small when it is used for small output power. Tab 1 is integrally formed with external

connection pins that become collector pins 3. Heat dissipation plate 4 is integrally formed with two collector pins 3.

[10] What is noteworthy here is the size of the aforesaid heat dissipation plate 4.

[11] To explain, the two side portions of heat dissipation plate 4 is larger than collector pins 3 by width W, and thus [the heat dissipation plate] is larger than distance *l* between the two pins. Because the heat dissipation plate 4 is large, its surface area becomes large, and the heat dissipation effect is improved.

[12] 5 is an external connection pin that becomes the emitter pin, and 6 is an external connection pin that becomes the base [pin].

[13] In the said external connection pins 3, 4 and 5, grooves 7, 8 and 9 are formed where package 21, further explained below, becomes engaged. Furthermore, by providing empty space 10 on the lead frame, the engagement between the upper and lower resin that forms the package is improved, and moisture intrusion is reduced, enhancing moisture resistance. Furthermore, notches 11, 12 formed in external connection pins 5, 6 prevent external connection pins 5, 6 from becoming disengaged. The bonding pad (not shown) that is formed on semiconductor chip 2 and the aforesaid external connection pins 5, 6 are connected by wire bondings 13, 14 as shown in FIG. 2.

[14] Resin and the like is molded around [the structure] as shown in FIG. 2 to become a package 11 shaped, for example, as shown in FIG. 3.

[15] A transistor with the afore-described structure has an exceptionally good heat dissipation effect and can be fully used even in electronic circuits where an output power of 1 W or higher is needed. Also, by providing the aforesaid grooves 7, 8 and 9, the moisture penetration path for moisture working its way into package 21 via the external connection pins 3, 5 and 6 is made longer, improving moisture resistance.

Embodiment 2

[16] A second embodiment of the present invention is described next with reference to FIG. 4a. The same numbers are used for the same parts in the first and the second embodiments of the present invention, and redundant description is not provided.

[17] As FIG. 4a shows, heat dissipation plates 4a and 4b are individually provided to the two external connection pins 3. The heat dissipation plates 4a and 4b are each bent outwardly. The heat dissipation plates 4a, 4b are cut at the position of dotted line A in FIG. 1 and are then bent. The sum of the areas is equal to that of afore-described heat dissipation plate 4.

[18] FIG. 4b and FIG. 4c show embodiments of heat dissipation plates that are larger than the heat dissipation plate shown in FIG. 1.

[19] By forming heat dissipation plates 4a, 4b with a bent construction, two transistors of the same structure, which are mounted adjacent to each other, are prevented from experiencing an unexpected contact between the heat dissipation plates, i.e., an unexpected contact between a collector and another collector.

Embodiment 3

[20] A third embodiment of the present invention is described next with reference to FIG. 5. This embodiment shows the application of the present invention to a dual inline IC.

[21] As FIG. 5 shows, a heat dissipation plate 32 is formed on two external connection pins 31. The heat dissipation plate 32 may be disposed on a pin that is connected to the tab (not shown) or may be disposed on a pin where a high current flows such as the output circuit. Furthermore, the

position is not limited to the illustrated position, and a different position may be used. By disposing a heat dissipation plate 32 of a large size, heat generated by the semiconductor chip (not shown) is efficiently dissipated.

Effects

[22] (1) By using the external connection pins of a semiconductor device and forming a large heat dissipation plate, heat is efficiently dissipated from a semiconductor chip, allowing a semiconductor device of a high output power to be driven.

[23] (2) By disposing a heat dissipation plate on an external connection pin, the mechanical strength of the external connection pin is increased, reducing undesired deformation of the external connection pin and increasing the efficiency of the mounting work.

[24] Although the invention by the present inventors was described with reference to specific embodiments, the present invention is not limited to the afore-described embodiments, and needless to say, various modifications are possible without deviating from the gist of the present invention.

[25] For example, the heat dissipation plates 4a, 4b can be disposed on external connection pins used for the base and the emitter as shown in the second embodiment.

Field of Use

[26] Although, in the foregoing description, the field of use of the invention by the present inventors was primarily transistors and ICs, which is the background against which the invention was made, the field of use is not limited to them.

[27] For example, [the present invention] can be used with hybrid ICs.

Brief Description of the Figures

[28] FIG. 1 is a plan view showing the frame of a transistor exemplifying a first embodiment of the present invention.

[29] FIG. 2 is a perspective view showing the relationship between the aforesaid frame and a semiconductor chip.

[30] FIG. 3 shows an external view of the aforesaid transistor.

[31] FIGs. 4a, 4b and 4c show the external view of a transistor exemplifying a second embodiment of the present invention.

[32] FIG. 5 shows an external view of a dual inline IC exemplifying a third embodiment of the present invention.

1. Tab
2. Semiconductor chip
3, 5, 6, 31. External connection pin
4, 4a, 4b, 32. Heat dissipation plate
l. Length
W. Width
21. Package

Agent: Patent attorney Akio Takahashi

FIG. 1

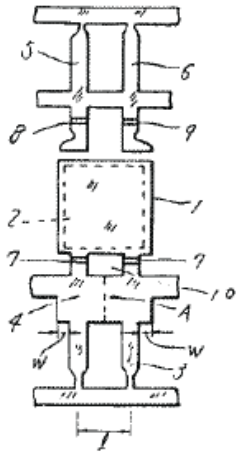


FIG. 2

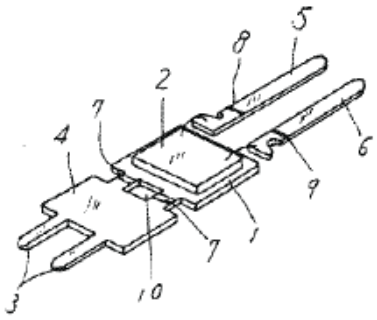


FIG. 3

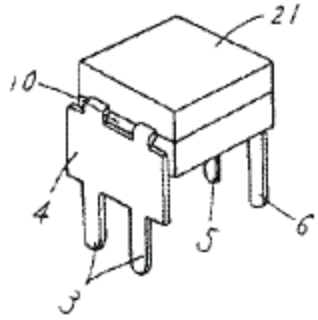


FIG. 5

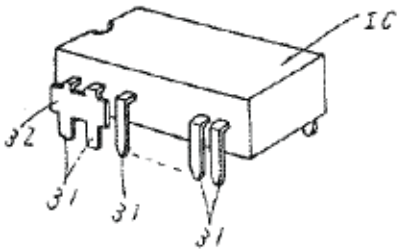


FIG. 4a

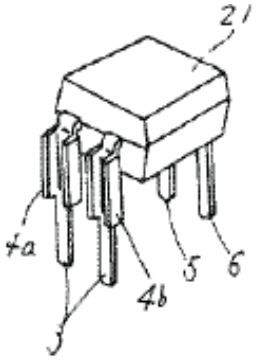


FIG. 4b

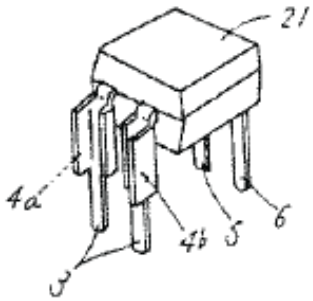
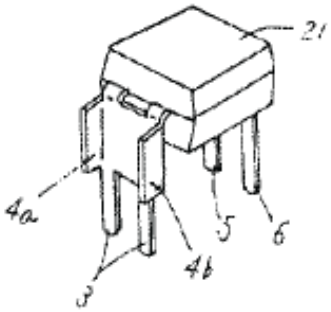


FIG. 4c



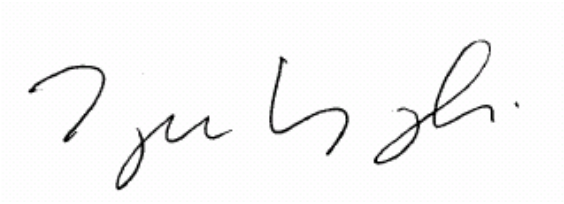
Toyu Yazaki
6348 Meadowridge Drive,
Santa Rosa, CA 95409

Telephone: (415) 505-0581
FAX: (772) 619-0664
e-mail: toyuyyaz@gmail.com

I, Toyu Yazaki, hereby declare that I am a professional interpreter and translator, with over twenty-five (25) years of professional experience, and am knowledgeable of and well acquainted with the Japanese language and the English language.

The document in the English language attached hereto is to the best of my ability, knowledge and expertise the correct English translation of JPA_1986080842 written in the Japanese language.

I declare under penalty of perjury under the laws of United States that the foregoing is true and correct. Executed this 5th day of August 2019 at Santa Rosa, CA.



Toyu Yazaki

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－80842

⑤1Int.Cl.⁴　識別記号　庁内整理番号　⑬公開　昭和61年(1986)4月24日
H 01 L 23/34　6616－5F

審査請求　未請求　発明の数 1　（全3頁）

⑤4発明の名称　半導体装置

⑳特　願　昭59－201747
㉒出　願　昭59(1984)9月28日

⑦2発明者　大高　成雄　高崎市西横手町111番地　株式会社日立製作所高崎工場内
⑦2発明者　榎本　宇佑　高崎市西横手町111番地　株式会社日立製作所高崎工場内
⑦2発明者　飯島　哲郎　高崎市西横手町111番地　株式会社日立製作所高崎工場内
⑦1出願人　株式会社日立製作所　東京都千代田区神田駿河台4丁目6番地
⑦4代理人　弁理士　高橋　明夫　外1名

明　細　書

発明の名称　半導体装置

特許請求の範囲

1. 外部接続端子に少なくとも2個の外部接続端子間の長さ以上の放熱板を形成したことを特徴とする半導体装置。

発明の詳細な説明

〔技術分野〕

本発明は半導体装置に関し、特に良好な放熱効果が要求される大出力電力用トランジスタ、半導体集積回路に用いて好適なものである。

〔背景技術〕

大出力電力用トランジスタを例に述べると、放熱効果が良好であるか否かによって出力電力が決定される、と言っても過言ではない。従って、半導体装置の放熱板については種々の提案がなされているのであるが、本発明者等は、出力電力が例えば1W以上にもなる出力用トランジスタの放熱を念頭におき、種々の技術的検討を行ない、本発明をなすに至った。

なお、特開昭57－177548号公報には、上記放熱板に関する提案がなされている。

〔発明の目的〕

本発明の目的は、外部接続端子を利用して放熱効果を良好に行ない得る半導体装置を提供することにある。

本発明の上記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

〔発明の概要〕

本願において開示される発明の概要を簡単に述べれば、下記のとおりである。

すなわち、トランジスタについて述べるとコレクタに接続される外部接続端子に2個の外部接続端子間の長さ以上の大放熱板を形成し、放熱効果を良好にする、という本発明の目的を達成するものである。

〔実施例－1〕

次に、第1図～第3図を参照して本発明を適用した半導体装置の第1実施例を述べる。なお、本

実施例では、大出力電力トランジスタへの適用例を述べる。

先ず、第1図についてフレームの構造から述べると、1はタブであり、その上面に点線で示すような半導体チップ2が設けられる。なお、半導体チップ2は大出力電力用の場合に点線で示すように大型になるが、小出力電力用の場合はその形状が小型になる。タブ1はコレクタ端子3となる外部接続端子と一体であり、2個のコレクタ端子3には放熱4が一体に形成されている。

ここで注目すべきは、上記放熱板4の大きさである。

すなわち、放熱板4の両側部はコレクタ端子3よりも幅Wだけ大であり、従って2個の端子間の長さℓよりも大となる。そして、放熱板4が大きくなった分につき、その表面積が大になり、放熱効果が良好になる。

なお、5はエミッタ端子となる外部接続端子であり、6はベースとなる外部接続端子である。

そして、上記外部接続端子3，4，5において、後述するパッケージ21に係合する部分には溝部7，8，9が形成され、さらにリードフレームには空間部10が設けられていることよりパッケージとなる、レジンの上下の食いつきを良くし水分の侵入を低減して防湿効果を向上するようになされている。また、外部接続端子5，6に形成された切り込み部11，12は、外部接続端子5，6の抜け止め用であり、半導体チップ2に形成されたボンディングパッド（図示せず）と上記外部接続端子5，6とは、第2図に示すようにワイヤボンディング13，14によって接続される。

そして、第2図に示す状態からレジン等によってモールドされ、第3図に示す如きパッケージ11の形状になされる。

上記構造のトランジスタによれば、放熱効果が極めて良好になり、1W以上の出力電力が要求される電子回路においても充分使用することができる。また、上記溝部7，8，9を設けることにより、外部接続端子3，5，6を伝わってパッケージ21内に侵入しようとする水分の侵入経路が大となり、耐湿性を向上させることもできる。

〔実施例－2〕

次に、第4図aを参照して本発明の第2実施例を述べる。なお、上記第1実施例と同一部分には同一の符号を付し、説明の重複をさけるものとする。

第4a図に示すように、2個の外部接続端子3には個別に放熱板4a，4bが設けられ、これらはそれぞれ外側方向に折り曲げられている。放熱板4a，4bは第1図に点線Aの位置で切断され、しかる後に折り曲げられたものであり、面積の和は上記放熱板4に等しい。

第4b図、第4c図は、第1図に示す放熱板より大きな放熱板を有する実施例の図を示す。

そして、放熱板4a，4bを折り曲げ構造にすることにより、同一構造のトランジスタを隣接して実装する場合に、放熱板と放熱板の接触、言い換えればコレクタとコレクタとの不測の接触を防止することができる。

〔実施例－3〕

次に、本発明の第3実施例を第5図を参照して述べる。なお、本実施例は、本発明をデュアルインライン型のICに適用したものである。

第5図に示すように、2個の外部接続端子31について放熱板32が形成されている。放熱板32は、例えばタブ（図示せず）に接続された端子に設けてもよく、或いは出力回路の如く大電流の流れる端子に設けてもよい。また、図示の位置に限定されるものではなく、他の位置に設けてよい。すなわち、大形状の放熱板32を設けることにより、半導体チップ（図示せず）から発生した熱を効率よく放熱させることができる。

〔効果〕

(1) 半導体装置の外部接続端子を利用して大形状の放熱板を設けることにより、半導体チップの放熱が効率的に行われるので、大出力電力で半導体装置を駆動することができる。

(2) 外部接続端子に放熱板を設けることにより、外部接続端子の機械的強度が増し、外部接続端子の不所望の変形が低減され、実装時の作業効率が

向上する。

以上本発明者によってなされた発明を実施例にもとづき具体的に説明したが、本発明は上記実施例に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

例えば、第2実施例に示す如き放熱板4a，4bをベース，エミッタ用の外部接続端子に設けてもよい。

〔利用分野〕

以上の説明では、主として本発明者によってなされた発明をその背景となった利用分野であるトランジスタ，ICについて説明したが、それに限定されるものではない。

例えば、ハイブリッドICに利用することができる。

図面の簡単な説明

第1図は本発明の第1実施例を示すトランジスタのフレームの平面図を示し、

第2図は上記フレームと半導体チップとの関係を示す斜視図を示し、

第3図は上記トランジスタの外観図を示し、

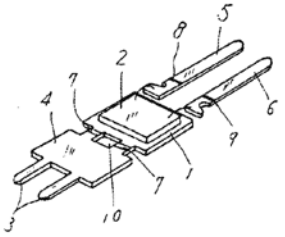
第4a図，第4b図，第4c図は本発明の第2実施例を示すトランジスタの外視図を示し、

第5図は本発明の第3実施例を示すデュアルインライン型ICの外観図を示す。

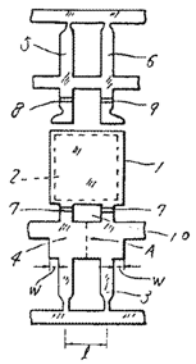
1…タブ、2…半導体チップ、3，5，6，31…外部接続端子、4，4a，4b，32…放熱板、ℓ…長さ、W…幅、21…パッケージ。

代理人　弁理士　高　橋　明　夫

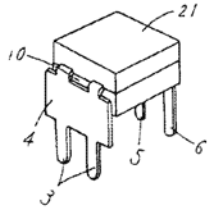
第　2　図



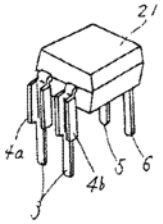
第　1　図



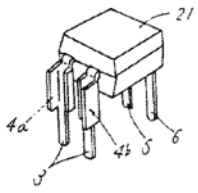
第　3　図



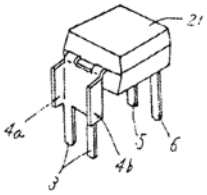
第　4a　図



第　4b　図



第　4c　図



第　5　図

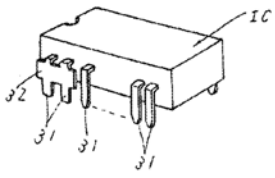


EXHIBIT 29

REDACTED IN ITS ENTIRETY

EXHIBIT 30

REDACTED IN ITS ENTIRETY

EXHIBIT 31

REDACTED IN ITS ENTIRETY

EXHIBIT 32

EXHIBIT 33

REDACTED IN ITS ENTIRETY

EXHIBIT 34

THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

ON SEMICONDUCTOR CORPORATION and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,	)	
Plaintiffs,	)	
v.	)	C.A. No. 17-247-LPS
POWER INTEGRATIONS, INC.,	)	
Defendant.	)	

DECLARATION OF ANDREW E. RUSSELL IN SUPPORT OF DEFENDANT POWER INTEGRATIONS, INC.'S MOTIONS FOR SUMMARY JUDGMENT

I, Andrew E. Russell, declare:

1. I am partner at the law firm of Shaw Keller LLP, counsel for Power Integrations, Inc. ("Power Integrations") in the above-captioned action. I am a member of the Bar of the State of Delaware (No. 5382). I have personal knowledge of the facts set forth herein, and if called upon to testify, I could and would competently testify to the statements made herein.

2. I offer the following statements regarding the exhibits in the appendix to Power Integrations, Inc.'s Motions for Summary Judgment.

3. Exhibit 7 is a true and correct copy of Japanese Unexamined Patent Application Publication No. S61-53752, and a certified translation thereof, as produced in this litigation with bates numbers added. The original Japanese-language document was obtained by downloading it from the Official Website of the Japan Patent Office. That document remains available from the Official Website of the Japan Patent Office, via the search function linked from https://www.jpo.go.jp/e/.

4. Exhibit 8 is a true and correct copy of Japanese Unexamined Patent Application Publication No. S62-45054A, and a certified translation thereof, as produced in this litigation with bates numbers added. The original Japanese-language document was obtained by downloading it from the Official Website of the Japan Patent Office. That document remains available from the Official Website of the Japan Patent Office, via the search function linked from https://www.jpo.go.jp/e/.

5. Exhibit 9 is a true and correct copy of Japanese Unexamined Patent Application Publication No. S62-206868, and a certified translation thereof, as produced in this litigation with bates numbers added, and with paragraph numbers added in brackets. The original Japanese-language document was obtained by downloading it from the Official Website of the Japan Patent Office. That document remains available from the Official Website of the Japan Patent Office, via the search function linked from https://www.jpo.go.jp/e/.

6. Exhibit 10 is a true and correct copy of Japanese Unexamined Patent Application Publication No. H4-225268, and a certified translation thereof, as produced in this litigation with bates numbers added. The original Japanese-language document was obtained by downloading it from the Official Website of the Japan Patent Office. That document remains available from the Official Website of the Japan Patent Office, via the search function linked from https://www.jpo.go.jp/e/.

7. Exhibit 28 is a true and correct copy of Japanese Unexamined Patent Application Publication No. S61-80842, as produced in this litigation with bates numbers added, and a certified translation thereof, with paragraph numbers added in brackets. The original Japanese-language document was obtained by downloading it from the Official Website of the Japan

Patent Office. That document remains available from the Official Website of the Japan Patent Office, via the search function linked from https://www.jpo.go.jp/e/.

8. Exhibit 11 is a true and correct copy of Chin C. Lee, David H. Chien, and Chen S. Tsai, "An Optimization Study of Thermal Path from Plastic Packages to Board," The International Journal of Microcircuits and Electronic Packaging, Volume 21, Number 1, First Quarter 1998 (ISSN 1063-1674), as produced in this litigation with bates numbers added. This document was obtained by downloading it from the website of The International Journal of Microcircuits and Electronic Packaging. This document remains available from the website of The International Journal of Microcircuits and Electronic Packaging, via the link at http://www.imaps.org/journal/1998/q1_1998.asp.

9. Exhibit 12 is a true and correct copy of excerpts from the affidavit of Christopher Butler, Office Manager at the Internet Archive (omitting material irrelevant to the present motions), as produced in this litigation, with bates numbers added. The original document was obtained by mail from Mr. Butler.

10. Exhibit 13 is a true and correct copy of a portion of the World Intellectual Property Organization Handbook on Industrial Property Information and Documentation, Standard ST.9 (June 2013), as cited in *Tokyo Electron Limited v. Daniel L. Flamm*, 2017 Pat. App. LEXIS 13067, at *24-27 (PTAB Oct. 4, 2017). This document was obtained by downloading it from the World Intellectual Property Organization website using the URL provided in the *Tokyo* opinion. The original document remains available from the World Intellectual Property Organization website, via the link at https://www.wipo.int/standards/en/part_03_standards.html.

11. Exhibit 18 is a true and correct copy of a printout from merriam-webster.com. The website remains available from the Merriam-Webster website, at https://www.merriam-webster.com/dictionary/extend.

12. Certain of the exhibits referred to above, and other exhibits in the appendix, have highlighting added for the Court's convenience, and all of the documents have appendix numbers added.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on August 5, 2019 in Wilmington, Delaware.

/s/ Andrew E. Russell

Andrew E. Russell (No. 5382)
SHAW KELLER LLP
I.M. Pei Building
1105 North Market Street, 12th Floor
Wilmington, DE 19801
(302) 298-0700
arussell@shawkeller.com
Attorney for Power Integrations, Inc.

Dated: August 5, 2019

CERTIFICATE OF SERVICE

I, John W. Shaw, hereby certify that on August 6, 2019, this document was served on the persons listed below in the manner indicated:

BY EMAIL

John G. Day
Andrew C. Mayo
ASHBY & GEDDES, P.A.
500 Delaware Avenue, 8th Floor
P.O. Box 1150
Wilmington, DE 19899
(302) 654-1888
jday@ashby-geddes.com
amayo@ashby-geddes.com

Roger Fulghum
BAKER BOTTS LLP
910 Louisiana
Houston, TX 77002
(713) 229-1707
roger.fulghum@bakerbotts.com

Brett J. Thompsen
Mark Speegle
Nicholas Schuneman
BAKER BOTTS L.L.P.
98 San Jacinto Blvd., Suite 1500
Austin, TX 78701
(512) 322-2500
brett.thompsen@bakerbotts.com
mark.speegle@bakerbotts.com
nick.schuneman@bakerbotts.com

Colette Reiner Mayer
MORRISON & FOERSTER LLP
755 Page Mill Road
Palo Alto, CA 94304
(650) 813-5600
crmayer@mofo.com

/s/ John W. Shaw
John W. Shaw (No. 3362)
Andrew E. Russell (No. 5382)
SHAW KELLER LLP
I.M. Pei Building
1105 North Market Street, 12th Floor
Wilmington, DE 19801
(302) 298-0700
jshaw@shawkeller.com
arussell@shawkeller.com
Attorneys for Defendant